# TABLE OF CONTENT

Chapter 1 Device and Reliability

<table>
<thead>
<tr>
<th>Title</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Improvement in Metal-Insulator-Metal Capacitor Reliability by Using TiN only Bottom Plate</td>
<td>1</td>
</tr>
<tr>
<td>B. B. Greenwood and J. Prasad</td>
<td></td>
</tr>
<tr>
<td>Investigation of Impact from HDP Process on Device Performance</td>
<td>7</td>
</tr>
<tr>
<td>Ming Yuan Liu, Chia Chu Kuo, Wen Guang Zhang and Chung Li Fan</td>
<td></td>
</tr>
<tr>
<td>The Effect of Post-Metallization Annealing on the Reliability of Copper Interconnects</td>
<td>13</td>
</tr>
<tr>
<td>Jeff Gambino, Tom C. Lee, Dave Meatyard, Steve Mongeon, Baozhen Li and Fen Chen</td>
<td></td>
</tr>
<tr>
<td>Origin of Frequency Dispersion in High-K Dielectrics</td>
<td>20</td>
</tr>
<tr>
<td>P. Taechakumput, C. Z. Zhao, S. Taylor, M. Werner, P. R. Chalker, J. M. Gaskell, A. C. Jones and M. Drobnis</td>
<td></td>
</tr>
<tr>
<td>High-K Materials and Their Response to X-Ray Radiation</td>
<td>27</td>
</tr>
<tr>
<td>C. Z. Zhao, S. Taylor, P. Taechakumput, M. Werner, P. R. Chalker, X. L. Huang, T. J. Greenshaw, J. M. Gaskell and A. C. Jones</td>
<td></td>
</tr>
<tr>
<td>Simulation Study on Gate-all-Around Cylindrical (GAAC) Transistor for Sub-10 Nanometer Scaling</td>
<td>33</td>
</tr>
<tr>
<td>Deyuan Xiao, Joseph Xie, Min Hwa Chi, Xi Wang and Yuehui Yu</td>
<td></td>
</tr>
<tr>
<td>Mechanism Study of Hot Carrier Induced Degradation in LDMOSFET</td>
<td>43</td>
</tr>
<tr>
<td>Xinggong Wan, Xiangming Xu, Yi Tang and Zhao Hong Lv</td>
<td></td>
</tr>
<tr>
<td>Charge to Breakdown of ONO, the Bottom Oxide and the Top Oxide in ONO for NROM™ Applications</td>
<td>48</td>
</tr>
<tr>
<td>Feng Yan, Yong Zhao, Dan Liu, Joshua Wang, Yiqiang Hu and Zhaoyong Lu</td>
<td></td>
</tr>
<tr>
<td>Case Study for Mushroom Defect Encountered at Passivation Module</td>
<td>52</td>
</tr>
<tr>
<td>K. A. Mohammad, S. F. Liew, D. G. Lee, S. F. Chong and W. L. Liu</td>
<td></td>
</tr>
<tr>
<td>Simulation on the Effect of Halo Implantation Precision on the Performance of 36nm NMOSFET Device</td>
<td>58</td>
</tr>
<tr>
<td>Jianwen Qi, Xiulan Cheng and Masayasu Tanjyo</td>
<td></td>
</tr>
<tr>
<td>Equivalent Circuit Analysis of V-SrZrO3 Sputter-Deposited Thin Films Showing Resistive Switching</td>
<td>64</td>
</tr>
<tr>
<td>ESD Protection Design for RF Circuits in CMOS Technology with Low-C Implementation</td>
<td>70</td>
</tr>
<tr>
<td>Chun-Yu Lin and Ming-Dou Ker</td>
<td></td>
</tr>
<tr>
<td>Positive Charge in HF-Based Dielectric Stacks</td>
<td>76</td>
</tr>
<tr>
<td>J. F. Zhang, C. Z. Zhao and M. H. Chang</td>
<td></td>
</tr>
</tbody>
</table>
Stress Simulation of Embedded Si$_1$-$x$C$_x$ Source/Drain nMOSFETs........................................88
A. Biswas, M. Bargallo Gonzalez, A. De Keersgieter, E. Simoen, G. Eneman, P. Verheyen and C. Claeys

High Voltage P-Channel MOSFET for RF Applications..................................................93
Jinshu Zhang, Dumitru Sdrulla, Dahwen Tsang, Dick Frey and George Krausse

A New Analytical Subthreshold Behavior Model for Asymmetrical Dual Material
Double-Gate (ADMDG) MOSFET's ..................................................98
T.K. Chiang and T.H. Chiang

Electromigration and Signal Integrity in Multilevel Interconnection..............................106
Jianjun Wei and Xiaoping Huang

A New Self-Aligned BOI (Body-on-Insulator) FinFET Fabricated on Bulk Si Wafers ..................112
Runsheng Wang, Xiaoyan Xu, Jing Zhuge, Gang Chen, Wenhua Wang, Xing Zhang, Yangyuan Wang and Ru Huang

Reliability Enhancement in Advanced MOSFETs Using the U-Shape STI Structure for
Radiation Application.................................................................119
Yunpeng Pei, Xia An and Ru Huang

A New Measurement Method on 1/F Noise of Wafer Level........................................124
L.H. Huang, Y.G. Zhao, N. Sa, B. Zhao, J.Q. Yang and J. F. Kang

Properties of Ballistic Current in MOSFETs Studied by RT Model..................................129
Yasuhiro Morozumi, Kuniyuki Kakushima, Parhat Ahmet, Kazuo Tsutsui, Nobuyuki Sugii, Takeo Hattori, Kenji Natori and Hiroshi Iwai

Chapter 2 Design for Manufacturing(DFM)

The Roll of CMP Modeling in DFM..................................................................................133
Li Song, Kuang Han Chen and Taber Smith

Three-Dimensional Electromagnetic Modeling of System-in-Package and
System-on-Glass Transmission-Line Parameters for DFM............................................138
Keh-Jeng Chang, Tsun-Ming Wu, and Ming-Jin Huang

Implications of Variability on Timing, Power, Reliability and Yield at 45nm and
Beyond.......................................................................................144
Jamil Kawa and Charles Chiang

Efficient Atomistic Method Simulation on Low Energy Doping and High Temperature
Annealing Technology...............................................................149
Min Yu, Huihui Ji, Li Yuan, Ming Li, Ru Huang and Xing Zhang

Impacts of Gate Line Edge Roughness on Sub 100nm MOSFETs.................................155

Chapter 3 Photolithography
Advanced Scanner Focus Off-Line Monitor with Optical Scatterometry
Lisa Qin, Andy Shu, Nancy Liu, Oliver Li and Alien Lin
65nm Intermetal Layer Litho Performance Optimization by Plasma Treatment
Petros An, JK Seo, Oliver Li and Alien Lin
Status and Challenges of Template Fabrication Process for UV Nanoimprint Lithography
Masaaki Kurihara
Current Status of Immersion Exposure Tool
Takashi Masuyuki and Motokatsu Imai
Study for Trench Double Patterning Process under Limited Illumination System
CI Choi, Miller Qiu, Winter Li, Hans Sui and Fumitake Mieno
Novel Registration Control Method with Patterning Induced Stress Release Model for Beyond 65nm-Node Lithography
Dong-Il Park, Yoon-Young Chang, Jun-Sik Cho, Lee-Ju Kim, Chang-Nam Ahn and Hong-Suk Kim
Formulating for Extreme PR-Stripping, Achieving Performance, Selectivity, Stability
John Moore
An Extreme Ultraviolet Lithography Procedure for the Fabrication of Passive Crossbar Arrays
Xinghua Liu, Ming Liu, Changqing Xie, Deyu Tu, Xiaoli Zhu, Liwei Shang, Lijuan Zhen and Ge Liu
Molecular Glass Photoresists Based on Acidolysis of Acetal Compounds
Liyuan Wang, Xiaoxiao Zhai, Zhanxing Chu and Long Cheng
Automatic Optimization of MEEF-Driven Defect Disposition for Contamination Inspection Challenges
Tracy Huang, Aditya Dayal, Kaustuve Bhattacharyya, Joe Huang, William Chou, Yung-Feng Cheng, Shih-Ming Yen, James Cheng and Peter Peng
Study on Major Contributions to OPC Inaccuracy in 180-nm Technology Node
Kim Wan Ho, Yet Ek Jen, Goh Pau Ying, Kang Jeong Tae and Lee Boon Chun
Influence of Substrates and Pretreatment on Adhesion Contact Angle as a Method for Litho Process Improvement
XiaoBo Guo, Ramoz Hii, ChuYaw Liau, SiewIng Yet, JeongTae Kang and BoonChun Lee
Controlling Resist Residue Defects at I-Line Poly Layer
Ng Wah Hoo, Yet Siew Ing, Liau Chu Yaw, Kang Jeong Tae and Lee Boon Chun
Dual Side Post Etch Overlay in Through Wafer Etching
H. W. van Zeijl, P. M. Sarro and N. Launay
Novel Developer-Soluble Anti-Reflective Coatings for 248-nm Lithography
Joyce Lowes, Ramil Mercado, Jim Meador, Chris Cox and Douglas Guerrero
Impact of Pattern Dependent Photoacid Diffusion to the Process Window under Low K1 Conditions .................................................. 260
  Lei Wang, Kaiming Ning, Peng Wu, Qingqing Wenren, Jun Zhu and Qiang Wu

BARC for Immersion and Hyper Na Process .................................................. 267
  Takahiro Kishioka, Rikimaru Sakamoto, Daisuke Maruyama, Yoshiomi Hiroi, Takuya Ohashi, Tomohisa Ishida, Shigeo Kimura, Hisayuki Watanabe and Yasuyuki Nakajima

Study of Pattern Transfer Quality for Nanoscale Lithography ................................. 271
  Jing-Jou Tang, Tzyy-Kuen Tien and Li-Yang Wang

Method for In-SITU Measuring Even Aberrations of Projection Optics in Lithographic Tools by Use of Optimized Phase-Shifting Marks .......................... 278
  Qiongyan Yuan, Xiangzhao Wang and Zicheng Qiu

Object-Based Mask Synthesis Algorithm Using Inverse Lithography Technique for 65nm-Node Technology .................................................. 287
  Wei Xiong, Jinyu Zhang, Min-Chun Tsai, Yan Wang and Zhiping Yu

Adaptable OPC for Double Patterning Technology .............................................. 293
  Yijjie Pan and Hongbo Zhang

A Study of Overlay Measurement Limit on Substrates with Varing Signal Qualities .................................................. 303
  Ying Zhang, Qiang Wu and Wei Mao

Chapter 4 FEOL & BEOL Advanced Processing

Control of Metal Gate Oxidation in Plasma Processing of IC Devices ................................. 311
  Songlin Xu and Li Diao

Productivity Improvement: First Wafer Effect of Poly/Tungsten-Silicide Stack for Sub-100nm Dram Application .................................................. 317
  Zhibiao Zhao, Andrew Kuo and Chuck Chung

Annealing of Neodymium Aluminate High-K Dielectric Deposited by Liquid Injection MOCVD Using Single Source Heterometallic Alkoxide Precursor ................................. 322
  Pouvanart Taechakumpit, Ce Zhou Zhao, Stephen Taylor, Matthew Werner, Nam Pham, Paul R. Chalker, Robert T. Murray, Jeffrey M. Gaskell, Helen C. Aspinall and Anthony C. Jones

New Method on Uniformity Tuning of Ta(N) Barrier Layer ......................................... 327
  Liu Yang, Jerry Xu, Liang Huang, Shan Wang and Jian Kang

A Highly Effective Shallow Trench Isolation Gap-Fill(Sti-Gap-Fill) Technology Using H2-Etch Enhanced HDP-CVD Process for 90nm Flash ......................................... 331
  Qingshan Li, Steed Xiao, Ji Li, Grace Ning, Yu Zhang, Wenxian Zhu and Jason Tian

SAVCD USG Integration in Advanced Flash Self-Align ............................................. 339
  Jennifer Jing, Rocky Zou, Oliver Xiang, Lily Jiang and Johnny Ji
An Effective Method for Micro-Arcing Detection in Encore Ta Process
B.B. Ni, Charles Xing, T.M. Lye and H. Zhou

A Study of the Impact of Substrate Temperature on the Post-Etch Valcano Defect
Jiwei Zhang, Charles Xing, Baibing Ni, Ronnie Jiang, Purp Sun, Paul He, Richard Ma, Tongmeng Lye and Hua Zhou

The Combination of Thermal No-Annealing and DPN Process to Form a Novel Sion Gate Dielectric for 65nm Technology Node and Beyond
Yonggen He, Jared Kuo, JianHua Ju, Yunzhen Liu, Youfeng He and YongJian Wu

Rapid Thermal Processing from 100 °C to 1100 °C without Lamps: Isothermal Cavity Concept and Process Results
Woo Sik Yoo, Igor J. Malik, Michel Ouaknine and Takashi Fukada

Environmental Challenges to China's Semiconductor Manufacturing Industry-AMC Effects to Semiconductor IC Fabrication in China
Richard Ma, Charles Xing, Johnson Lin, Sam Lin, Kevin Hung, Squarel Du and Hua Zhou

Diffusion Furnace Dopant Activation Matching through a Ramped Temperature Idle
Kevin Black

A Metrology of Semiconductor BEOL Nanotechnology Lithography and Gap Fill Processes Integration
Chun-Jen Weng, Wen-Kuan Yeh and Chia-Chih Ou

Process Development and Optimization of Non-Fluorine HDI Resist Strip at 45nm
K. Han, S. Luo, P. Geissbühler, Q. Han, I. Berry, R. Sonnemans, V. Grimm and C. Krueger

Novel Approach for a New Post Etch/Ash Residue Removal
Libbert Peng, Bing Liu, Andrew Wang, David Yin and Shumin Wang

An Analysis of the Ball Type Defect Formation Mechanism in Encore Ta Process
Andy Chen, Wanghui, Charles Xing, T.M. Lye, Richard Ma and Hua Zhou

Impact of Ion Implantation on Nickel Germanides Formation with Pure-Ge Substrate and the Electrical Dependence of NiGe/Ge Schottky Diode on Contact Size
Xia An, Chunhu Fan, Ru Huang and Xing Zhang

Characterization of ZnO-DOPED Zr0.8Sn0.2TiO4 Dielectric Thin Films by SOL-GEL Method
Cheng-Hsing Hsu, Chun-Hung Lai, Yi-Mu Lee, Ching-Fang Tseng and Ching-Yi Chung

Advanced and Challenges in Post Salicidation Cleans for 45nm Technology Node and Beyond

Critical Issues in Flow Control for Advanced Semiconductor Processing
Hubert Dinh, Renny Reed, Mohamed Saleem and Sowmya Krishnan
Roadblocks and Critical Aspects for Sub 45nm Wafer Cleaning and Possible Solutions


X-Ray Diffraction and Annealing Study of Aluminum Thin Film

Ping Linda Zhang, Ping Huang and Zhongyuan Jin

UV Assisted Thermal Curing: Overview and Fundamental Understanding through Spin-on and PECVD Processes

Aziz Zenasni, Vincent Jousseau, Olivier Gourhant, Laurent Favennec and Patrick Maury

Schottky-Barrier-Height Modulation of Ni Silicide/Si Contacts by Insertion of Thin Er or Pt Layers

Yoshihisa Ohishi, Kohei Noguchi, Kuniyuki Kakushima, Parhat Ahmet, Kazuo Tsutsui, Nobuyuki Sugii, Takeo Hattori and Hiroshi Iwai

Review of Low-K Dielectric Constant Materials

Huiling Shi, Baimei Tan, Wei Sun and Lihui Hou

The Cleaning Method Which is Able to Keep the Smoothness of Si(100)

Xiang Li, Xin Gu, Akinobu Teramoto, Rihito Kuroda, Rui Hasebe, Tomoyuki Suwa, Ningmei Yu, Shigetoshi Sugawa, Takashi Ito and Tadahiro Ohmi

Impacts of Poly-Si Gate Pre-Implanted Dopant on the Performance and HCI Reliability of 65nm NMOS Device

Jie Huang and Yandong He

The Material Characterization of Nickel Germanosilicides on SiGe/Si Substrate and the Contact Size Effect on Schottky Diodes

Chunhui Fan, Xia An and Ru Huang

Damascene Metal Gate Technology for Damage-Free High-K Process Integration

Ralf Endres and Udo Schwalke

Advanced Inline Process Control on PVD System-An Application of RGA for IC Manufacturing Quality and Capacity Improvement

Yong-Qiang Wu, Ping Huang, Xing-Hua Song, Yi-Hui Lin, Xi-Peng Wang, Hsueh-Hung Wei, Huang-Her Yang and Paul-Chang Lin

PNL Application on WCVD Process-Contact Step Coverage Optimization for 0.13um Logic Products Yield Improvement

Dong Ouyang, Xiang-Tao Kong, Kun Gui, Jun Ji, Xiao-Bo Li, Chi-Hsien Peng and Paul-Chang Lin

Cluster Ion Implantation System for Beyond 45nm Device Fabrication

Masayasu Tanjyo, Nariaki Hamamoto, Tsutomu Nagayama, Sei Umisedo, Yuji Koga, Noriaki Maehara, Hideyasu Une, Takao Matsumoto and Nobuo Nagai

Chapter 5 CMP and Post-CMP Cleaning
Opportunities and Challenges in Electrochemical-Mechanical Planarization (ECMP) .......................................................... 511
A. Muthukumaran, N. Venkataraman, S. Raghavan and M. Keswani

Integration Solution for a 300mm Direct STI CMP Process Qualification for 65nm Logic Product .......................................................... 518
Xucheng Wang, Pengfei Li, Tony Wang and Shan Wang

Investigation of Post CMP Voids in Narrow Trenches of 65nm Technology Node .......................................................... 522
Ruipeng Yang, Jiaxiang Nie, Yun Kang, Weiye He, Na Su, Paolo Bonfanti and Yuhui Hu

Cu/Barrier CMP Protection Film Characterization Using Electrochemical Technique .......................................................... 526
Sunny Xu and Shumin Wang

Evolution and Revolution of Cerium Oxide Slurries in CMP .......................................................... 531
David Merricks, Brian Santora, Bob Her and Craig Zedwick

Corrosion and Organic Defects during Chemical Mechanical Polishing of Copper .......................................................... 537
Zhendong Liu, Robert Schmidt and Hugh Li

Development of Acidic Post-CMP Cleaners for Tungsten CMP .......................................................... 543
D. Tamboli, P. Subramanian, M. Rao and G. Banerjee

A New Ceria-Based ILD CMP Slurry .......................................................... 549
Kai Luo, Zhan Chen, and Chul Woo Nam and Robert Vacassy

A Technical Approach of High Removal Rate Copper Slurry for 3D-IC and MEMS .......................................................... 556
Yoshiyuki Matsumura, Takashi Hirao, Akira Isobe and Masaharu Kinoshita

Developing a Single Dispersion for CMP of Copper and Barrier Layers .......................................................... 561
S. V. S. B. Janjam, V. V. S. C. Surisetty, S. Pandija, D. Roy and S. V. Babu

Study on Barrier CMP Slurry .......................................................... 569
Jery Chen, Peter Song, Shumin Wang and Chris Yu

Fundamental Characterization of Diamond Disc, Pad, and Retaining Ring Wear in Chemical Mechanical Planarization Processes .......................................................... 576
Y. Zhuang, L. Borucki and A. Philipossian

Investigation of Dynamic CMP Pad-Wafer Contact Characteristics by Computational Modeling .......................................................... 586
Bo Jiang and Gregory Muldowney

Study on CMP Mechanism and Nanometer Slurry of NiP Substrate of Computer Hard-Disk .......................................................... 592
Tian Jun Liu Yuling, Niu Xinhuan and Tan Baimei

Chapter 6 Packaging, Assembly and Test

Innovative Bonding Tool Design for Fine Pitch Copper Wire Applications .......................................................... 597
Giyora Gur and Langut Ilan
Packaging of Silicon Carbide Power Semiconductor Devices
Simon S. Ang, William D. Brown, Habib Mustain, Brian Rowden, Juan C. Balda and Alan Mantooth

Comparing Measurement Methods for Intermetallic Coverage
Tomer Levinson and Alon Menache

Microstructural Evaluation of Al-Cu Interfaces in Wire-Bonding
M. Drozdov, G. Gur, Z. Atzmon and W.D. Kaplan

Process Optimization for Ultra-Fine Pitch Wire Bonding
Horst Clauberg, Bob Chylak, Gary Schulze and Alan Slopey

Thermal Aging Study at 150 °C and 200 °C: Gold Ball Bonds to Aluminium Bond Pad

Chapter 7 Emerging Technology

Environmental Challenges and Opportunities in Nanoelectronics Manufacturing
Farhang Shadman

Plasma Etching of Nanometer-Scale Self-Assembled Features
Ying Zhang, Charles T. Black, Ho-Cheol Kim, Edmund M. Sikorski and Bang To

GST Thin Film Metrology with XRR and XRF
Mengqi Ye, Vignesh Ramakrishnan, A. F. Bello and H. Takahara

Novel Silicon MEMS Fabrication Processes including Anodic Bonding of Extremely Thin (60m –Thick) Silicon Film on Glass Substrate
Takayuki Nara, Kouki Oku, Yoshifumi Fukai, Hideki Hatagouchi and Yasushiro Nishioka

Novel Cu Alloy Seed Layers for Barrierless Metallization
Jinn P. Chu and C. H. Lin

Ruthenium Film Growth from Ru (CO)₃(C₆H₈) at Low Temperatures in Sequentially Pulsed Deposition Mode
V.Yu. Vasilyev, S.H. Chung and Y.W. Song

Deep Trech Etching for Through-Silicon Vias in Three-Dimensional Integrational Integration Technology
Jun Liang, Hirokazu Kikuchi, Takayuki Konno, Yusuke Yamada, Takaumi Fukashima, Tetsu Tanaka and Mitsumasa Koyanagi

Solution Processed Organic Memory Devices
Keryn Lian and Jie Zhang

Removal of Organic Contaminants on Si Wafer Surfaces by Electrochemical Cleaning Technique
Jianxin Zhang, Yuling Liu, Baimei Tan, Xinhuan Niu and Yanyan Huang
Carbon Nanotube for High Performance Flexible Electronics .......................... 690
  Qing Cao, Coskun Kocabas and John A. Rogers

Structure and Surface Control of Porous Silicon for Sensor Applications .......... 697
  Jingmei Lu and Xuan Cheng

Resistive Switching Characteristics of Hafnium Oxide with Cu Doping for
Nonvolatile Memory Application ........................................................................ 703
  Weihua Guan, Shihing Long, Ming Liu and Wei Wang

The Induced Effect in the Pt/BFO/BNDT/Pt Capacitors for the Application in
FERAM .................................................................................................................. 709
  Yongyuan Zang, Dan Xie, Tianling Ren, Litian Liu and Zhijian Li

Electrical Resistive Switching in Organic Molecules and High-K Dielectric Bi-Layer
Films ..................................................................................................................... 717
  Deyu Tu, Ming Liu, Liwei Shang, Xinghua Liu and Changqing Xie

Nano-Crystal Formation and Characterization for Memory Applications .......... 723
  Hua Ji, Hua-long Song, Yan Liu, Yong-gang Feng, Fu-xiong Zhang, Yang-hui Xiang,
  Mieno Fumitake, Min-hwa Chi, Jian-li Cui, He-yin Li, Lu Yu and Jia-nou Shi

Author Index ......................................................................................................... 729
Keyword Index ..................................................................................................... 735