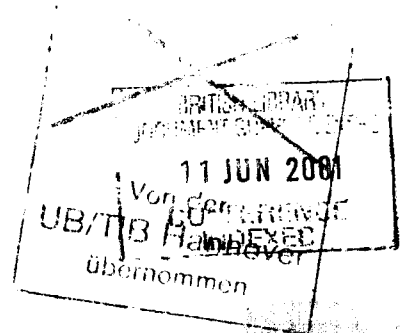


Proceedings

The International VHDL Conference

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Table of Contents

Message from the General Chair	vi
1999 HDL Conference Matrix	vii
Steering Committee	viii
Program Committee	ix
HDL 1999 Best Paper Award Winner	x
Keynote Speaker: Hector de J. Ruiz	1
Session 1: Intellectual Property	
<i>Session Chair: Paul Menchini, OrCAD, Durham, NC</i>	
1.1 Retargeting an IP Core to FPGA - An Efficient Approach	5
<i>Dattatri Mattur and Mahesha S - Integrated Intellectual Property, Inc., Santa Clara, CA</i>	
1.2 A Methodology for Multi-Lingual IP Authoring	11
<i>Sashi Obilisetty - DualSoft LLC, Nashua, NH</i> <i>Mahesh Girkar - Consultant, Nashua, NH</i>	
Session 2: Timing Issues	
<i>Session Chair: Tony O'Conner, Avid Technology, Inc., Tewksbury, MA</i>	
2.1 Negative Constraints: Issues with VITAL/Verilog	19
<i>Ravi S. Kumar - Interra, Inc., San Jose, CA</i>	
2.2 Correct Methods for Adding Delays to Verilog Behavioral Models	23
<i>Clifford E. Cummings - Sunburst Design, Inc., Beaverton, OR</i>	
2.3 Fundamental Principles of Modeling Timing in Hardware Description Languages for Digital Systems	30
<i>Sumit Ghosh - Arizona State University, Tempe, AZ</i>	
Panel 1: RTL Design Planning and Prototyping: Are We There Yet?	40
Session 3: VHDL Design Experiences	
<i>Session Chair: Praveen Chawla, EDaptive Computing, Inc., Dayton, OH</i>	
3.1 VHDL Design of an Intelligent Fuzzy Logic Controller for Synchronous Generator Sets Implemented in FPGA	43
<i>M. Cirstea, J. Khor, M. McCormick - De Montfort University, Leicester, UK</i> <i>L. Haydock - Newage International Ltd., Stamford, UK</i>	
3.2 A VHDL Modelling of a Digital Modem for LEO Satellite Communication: from FPGA-based Prototyping to ASIC Implementation	48
<i>Narcis Simon, Juanjo Noguera, Carles Ferrer - CNM-UAB, Bellaterra, Spain</i>	
3.3 Ethernet LAN Modeling with VHDL	55
<i>Reza Purtoosi, Zainalabedin Navabi - University of Tehran, Tehran, Iran</i>	

Session 4: Verilog Synthesis

Session Chair: Mike Ciletti, University of Colorado, Colorado Springs, CO

- 4.1 FSMDesigner: Combining a Powerful Graphical FSM Editor and Efficient HDL Code Generation with Synthesis in Mind 63
Lars Rzymianowicz - University of Mannheim, Mannheim, Germany
- 4.2 A Standard for Verilog HDL RTL Synthesis 69
J. Bhasker - Cadence Design Systems, Inc., Allentown, PA
- 4.3 Blocking and Non-Blocking Assignments in Explicit and Implicit Style Verilog Synthesis 71
Mark G. Arnold, Jerry J. Cupal - University of Wyoming, Laramie, WY
James D. Shuler - SUNY College at Brockport, Brockport, NY

Panel 2: New Techniques to Boost Functional Verification Efficiency..... 80

Session 5: Co-Simulation

Session Chair: Mike Baird, Willamette HDL, Inc., Beaverton, OR

- 5.1 An Experience Using a New Methodology for the Codesign of Embedded Hw/Sw Systems 83
Vincenza Carchiolo, Michele Malgeri, Giuseppe Mangioni – University of Catania, Catania, Italy
- 5.2 Hardware/Software Co-Simulation on Dual Processor NT Workstations 91
Ray Khorram - Pixel Magic, Inc., Andover, MA
- 5.3 Hardware/Software Co-Simulation Methodology Based on Two Alternative Approaches 96
J. Kamaras, K. Pramataris, G. Lykakis, G. Stassinopoulos - National Technical Univ. of Athens, Athens, Greece

Session 6: Language Issues

Session Chair: David Barton, Intermetrics, Inc., Vienna, VA

- 6.1 A Dependency Graph for VHDL Design Files and Design Units and Its Application in a VHDL Design Environment 103
Wolfgang Ecker, Jochen Mades, Thomas Schneider, Andre Windisch, Ke Yang - Siemens AG, Munich, Germany
- 6.2 Communication and Synchronization Using Bounded Channels in SUAVE 111
Peter J. Ashenden, Robert Esser - University of Adelaide, Adelaide, Australia
Philip A. Wilsey - University of Cincinnati, Cincinnati, OH
- 6.3 VHDL for Synchronous Action Systems 119
Tiberiu Seceleanu - TUCS-Datacity, Turku, Finland

Panel 3: Design Reuse – Myth or Magic..... 128

Session 7: Verification

Session Chair: Aidan Herbert, Design Acceleration, Inc., San Jose, CA

- 7.1 System Verification Using Large Data Patterns with Two-Dimensional Verilog

· The Need for Non-Constant Indices.....	131
<i>Edward A. Chavez - Compaq Computer Corp., Houston, TX</i>	
7.2 An RTL Design Verification Linting Methodology.....	135
<i>Lionel Bening - Hewlett-Packard Co., Richardson, TX</i>	
7.3 Integrating Code Coverage Analysis Into a Large-Scale ASIC Design Verification Flow.....	141
<i>Dennis Abts - Silicon Graphics, Inc., Chippewa Falls, WI</i>	
Session 8: HDL Design Environment Issues	
<i>Session Chair: Greg Tumbush, Wright Patterson Air Force Base, Dayton, OH</i>	
8.1 HDL Model Packaging Using OMI.....	147
<i>Kathy McKinley, Andrew Wilmot - Cadence Design Systems, Inc., Chelmsford, MA</i>	
8.2 Quantifying Design Reuse: An HDL-Based Design Experiment.....	153
<i>Yutana Jawchinda, Hideaki Kobayashi - University of South Carolina, Columbia, SC</i>	
8.3 The Philosophy of MEADE, A Modular, Extensible, Adaptable Design Environment.....	159
<i>Gary Spivey - DOD, Ft. Meade, MD and University of Maryland, College Park, MD</i>	
<i>Kazuo Nakajima - University of Maryland, College Park, MD</i>	
Author Index.....	167