Contents

Dedication v

1. INTRODUCTION 1
   1.1 Design Complexity 2
   1.2 The Design Productivity Gap 4
   1.3 The Verification Crisis 5
   1.4 Design Modeling and Verification 7
   1.5 Dynamic versus Static Verification 9
   1.6 Simulation 11
      1.6.1 Simulators 11
      1.6.2 Testbench 12
      1.6.3 Test Generation 12
      1.6.4 Checking Strategies 13
      1.6.5 Coverage 13
   1.7 Emulation 14
   1.8 Static Verification 15
      1.8.1 Equivalence Checking 15
      1.8.2 Model Checking and Bounded Model Checking 16
      1.8.3 Theorem Proving 17
      1.8.4 Language Containment 17
      1.8.5 Symbolic Simulation 17
      1.8.6 Hybrid Simulation and Formal Verification 18
   1.9 Constraints, Assertions, and Verification 18
      1.9.1 Constrained Random Simulation 19
      1.9.2 Assertion-based Verification 20
   1.10 A Composite Verification Strategy 20
4.2 Temporal Logic and Regular Expression 56
  4.2.1 Temporal Logic 57
  4.2.2 Regular Expression 58
  4.2.3 Truthness of Properties 59
  4.2.4 Strong and Weak Semantics 61
  4.2.5 Safety and Liveness Properties 63
  4.2.6 Multiple Paths and Initial States 65

4.3 Introduction to PSL 66
  4.3.1 The Four Layers of PSL 66
  4.3.2 Verification Units 66
  4.3.3 Sequential Extended Regular Expression 67
  4.3.4 The Foundation Language 68

4.4 Monitors and Generators 70
  4.4.1 Monitors 70
  4.4.2 Generators 73

4.5 Monitor Construction 74
  4.5.1 The Tableau Rules and Cover 75
  4.5.2 Constructing the NFA 76
  4.5.3 Determinization of NFA 79

4.6 Summary 80

5. PRELIMINARIES 83
  5.1 Boolean Algebra and Notations 83
  5.2 Graphs 84
  5.3 Hardware Modeling 85
  5.4 Reachability Analysis 88
  5.5 Reduced Ordered Binary Decision Diagrams 90
    5.5.1 BDD Representation of Boolean Functions 90
    5.5.2 BDD Manipulations 91
    5.5.3 The BDD Size Consideration 92
  5.6 Boolean Satisfiability 93
    5.6.1 SAT Solving 94
    5.6.2 Definitions 95
    5.6.3 Conflict-based learning and Backtracking 97
    5.6.4 Decision Heuristics 100
    5.6.5 Efficient BCP Implementation 101
    5.6.6 Unsatisfiable Core 102
    5.6.7 Other Optimizations 103
5.7 Automatic Test Pattern Generation 104
  5.7.1 The D-algorithm 105
  5.7.2 The PODEM and FAN algorithms 106

6. CONSTRATNED VECTOR GENERATION 109
  6.1 Constraints and Biasing 110
    6.1.1 BDD Representation of Constraints 110
    6.1.2 Input Biasing and Vector Distribution 111
    6.1.3 Constrained Probabilities 111
    6.1.4 An Example of Constrained Probability 112
  6.2 Simulation Vector Generation 113
    6.2.1 The Weight Procedure 114
    6.2.2 The Walk Procedure 115
    6.2.3 Correctness and Properties 117
  6.3 Implementation Issues 120
    6.3.1 Variable Ordering 120
    6.3.2 Constraint Partitioning 120
    6.3.3 The Overall Flow 121
  6.4 Variable Solve Order 121
  6.5 Weighted Distribution 124
  6.6 Cycling Variables and Permutations 125
  6.7 Historical Perspective 126
  6.8 Results 126
    6.8.1 Constraint BDDs 127
    6.8.2 A Case Study 128
  6.9 Summary 130

7. CONSTRAINT SIMPLIFICATION 133
  7.1 Definitions 135
  7.2 Syntactical Extraction 137
  7.3 Functional Extraction 139
  7.4 Constraint Simplification 142
    7.4.1 Recursive Extraction 143
  7.5 The Overall Algorithm 145
  7.6 Historical Perspective 145
  7.7 Experiments 148
    7.7.1 Impact on Building Conjunction BDDs 148
    7.7.2 Impact on Simulation 150
Contents

7.8 Summary 151
8. MORE OPTIMIZATIONS 153
  8.0.1 Constraint Prioritization 154
  8.0.2 Tree-decomposition 155
  8.0.3 Functional Decomposition 157
  8.0.4 Formula Factorization 158
8.1 Implication of Multiple Clocks 159
8.2 Summary 160
9. CONSTRAINT SYNTHESIS 161
  9.1 Problem Formulation 162
  9.2 The Constraint Synthesis Method 164
    9.2.1 Deriving Reproductive Solutions 165
    9.2.2 Don’t Cares 167
    9.2.3 Variable Removal 168
    9.2.4 The Overall Algorithm 169
  9.3 Other Synthesis Methods 170
  9.4 Coudert and Madre’s Method 171
    9.4.1 Randomization 174
  9.5 Building Circuits from Relations 175
    9.5.1 Computing the Weights 175
    9.5.2 Computing the Assignments 176
    9.5.3 Selecting the Outputs 177
  9.6 Synthesis using SAT solving 177
  9.7 Experimental Results 179
  9.8 Summary and Discussion 181
10. CONSTRAINT DIAGNOSIS 183
  10.1 The Illegal States 184
  10.2 Reachability Analysis 185
  10.3 Locating the Conflict Source 185
  10.4 Fixing Over-constraints via Illegal States Removal 186
  10.5 Summary 187
11. WORD-LEVEL CONSTRAINT SOLVING 189
  11.1 DPLL-based 01-ILP 192
    11.1.1 Linear Pseudo Boolean Constraints 193
    11.1.2 Cutting-planes in ILP 194
11.1.3 A DPLL-based 01-ILP Algorithm 196
11.2 Multi-valued Satisfiability 203
11.3 Word-level Constraint Solving 205
   11.3.1 Converting RTL to Integer Linear Constraints 206
   11.3.2 Propagation and Implication 211
   11.3.3 Lazy Evaluation 213
   11.3.4 Multiple Domain Reductions 214
   11.3.5 Conflict Analysis 214
   11.3.6 Arithmetic Solving 216
11.4 ATPG-based Word-level Constraint Solving 217
11.5 Randomization Consideration 220
11.6 Summary 220

Appendices 221
A Acronyms 221
B Proofs 223
   B.1 Proofs for Chapter 6 223
   B.2 Proofs for Chapter 7 226
   B.3 Proofs for Chapter 8 229

References 231

Index 247