<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming a hyper-programmable architecture for networked systems</td>
<td>1</td>
</tr>
<tr>
<td>Self-recovery experiments in extreme environments using a field programmable transistor array</td>
<td>9</td>
</tr>
<tr>
<td>Field programmable gate array implementation of a generalized decoder for structured low-density parity check codes</td>
<td>17</td>
</tr>
<tr>
<td>Partial character decoding for improved regular expression matching in FPGAs</td>
<td>25</td>
</tr>
<tr>
<td>Interconnect architectures for modulo-scheduled coarse-grained reconfigurable arrays</td>
<td>33</td>
</tr>
<tr>
<td>Directional and single-driver wires in FPGA interconnect</td>
<td>41</td>
</tr>
<tr>
<td>A greedy algorithm for tolerating defective crosspoints in NanoPLA design</td>
<td>49</td>
</tr>
<tr>
<td>SHAPER : synthesis for hybrid FPGAs containing PLAs using reconvergence analysis</td>
<td>57</td>
</tr>
<tr>
<td>Placement and routing for non-rectangular embedded programmable logic cores in SoC design</td>
<td>65</td>
</tr>
<tr>
<td>QuickRoute : a fast routing algorithm for pipelined architecture</td>
<td>73</td>
</tr>
<tr>
<td>An FPGA-based Othello endgame solver</td>
<td>81</td>
</tr>
<tr>
<td>Real-time detection of line segments using the line hough transform</td>
<td>89</td>
</tr>
<tr>
<td>gNBX - reconfigurable hardware acceleration of self-organizing maps</td>
<td>97</td>
</tr>
<tr>
<td>Evolvability and reconfigurability</td>
<td>105</td>
</tr>
<tr>
<td>A gate-level model for morphogenetic evolvable hardware</td>
<td>113</td>
</tr>
<tr>
<td>A novel CLB architecture to detect and correct SEU in LUTs of SRAM-based FPGAs</td>
<td>121</td>
</tr>
<tr>
<td>Using multi-bit logic blocks and automated packing to improve field-programmable gate array density for implementing datapath circuits</td>
<td>129</td>
</tr>
<tr>
<td>Stream applications on the dynamically reconfigurable processor</td>
<td>137</td>
</tr>
<tr>
<td>Compiler reuse analysis for the mapping of data in FPGAs with RAM blocks</td>
<td>145</td>
</tr>
<tr>
<td>Memory optimisations for high-resolution imaging</td>
<td>153</td>
</tr>
<tr>
<td>On the placement and granularity of FPGA configurations</td>
<td>161</td>
</tr>
<tr>
<td>Adaptive range reduction for hardware function evaluation</td>
<td>169</td>
</tr>
<tr>
<td>A scalable hardware architecture for prime number validation</td>
<td>177</td>
</tr>
<tr>
<td>Coarsely integrated operand scanning (CIOS) architecture for high-speed Montgomery modular multication</td>
<td>185</td>
</tr>
<tr>
<td>Programmable parallel coprocessor architectures for reconfigurable system-on-chip</td>
<td>193</td>
</tr>
<tr>
<td>Windows CE for a reconfigurable system-on-a-chip processor</td>
<td>201</td>
</tr>
<tr>
<td>EXPRESS-1 : a dynamically reconfigurable platform using embedded processor FPGA</td>
<td>209</td>
</tr>
<tr>
<td>Migrating software to hardware on FPGAs</td>
<td>217</td>
</tr>
<tr>
<td>The quartus university interface program : enabling advanced FPGA research</td>
<td>225</td>
</tr>
<tr>
<td>Maximizing system performance : using reconfigurability to monitor system communications</td>
<td>231</td>
</tr>
<tr>
<td>Using function folding to improve silicon efficiency of reconfigurable arithmetic arrays</td>
<td>239</td>
</tr>
</tbody>
</table>
Low FPGA area multiplier blocks for full parallel FIR filters  p. 247
Pipelining designs with loop-carried dependencies  p. 255
Reconfigurable hardware implementation of mesh routing in number field sieve factorization  p. 263
Fast architecture for FPGA-based implementation of RSA encryption algorithm  p. 271
Single-chip FPGA implementation of a cryptographic co-processor  p. 279
Reconfigurable implementation of bit-parallel multipliers over GF ($2^{(2^m)}$) for two classes of finite fields  p. 287
Extended genetic algorithm for codesign optimization of DSP systems in FPGAs  p. 291
FPGA implementation of hierarchical memory architecture for network processors  p. 295
Evaluating software and hardware implementations of signal-processing tasks in an FPGA  p. 299
Extended genetic algorithm for codesign optimization of DSP systems in FPGAs  p. 299
A scalable architecture for elliptic curve point multiplication  p. 303
An FPGA based prototyping platform of imager-on-chip applications  p. 307
Compact iterative FPGA camellia algorithm implementations  p. 311
An adaptive viterbi decoder based on FPGA dynamic reconfiguration technology  p. 315
Single bit error correction implementation in CRC-16 on FPGA  p. 319
Pre-silicon prototyping of a unified hardware architecture for cryptographic manipulation detection codes  p. 323
FPGA-acceleration of cone-beam reconstruction for the x-ray CT  p. 327
Interface adaptor logic - a new model for interfacing peripherals in IP based designs  p. 331
FPGA implementation of digital upconversion using distributed arithmetic FIR filters  p. 335
FPGA implementation of a phased array DBF using polyphase filters  p. 339
FPGA design of HECC coprocessors  p. 343
A tsume-shogi processor based on reconfigurable hardware  p. 347
An approach to realize time-sharing of flip-flops in time-multiplexed FPGAs  p. 351
A parameterizable HandelC divider generator for FPGAs with embedded hardware multipliers  p. 355
Reconfigurable I/O interface for mobile equipments  p. 359
Domain specific reconfigurable fabric targeting viterbi algorithm  p. 363
A new architecture of field programmable analog arrays for reconfigurable instantiation of continuous-time filters  p. 367
RTOS acceleration of soft-core processors using instruction set customization  p. 371
A rapid prototyping framework for audio signal processing algorithms  p. 375
Cyclic reconfiguration for pipeline applications on coarse-grain reconfigurable circuits  p. 379
Achieving wide frequency range in an analog FPGA  p. 383
3D graphics accelerator platform for mobile devices  p. 387