Preface
Acknowledgments
Introduction
Test and Design-for-Test Fundamentals
Introduction to Test and DFT Fundamentals
Purpose
Introduction to Test, the Test Process, and Design-for-Test
Concurrent Test Engineering
The Reasons for Testing
Why Test? Why Add Test Logic? Pro and Con Perceptions of DFT
The Definition of Testing
What Is Testing? Stimulus
Response
Test Measurement Criteria
What Is Measured? Fault Metric Mathematics
Fault Modeling
Physical Defects
Fault Modeling
Types of Testing
Functional Testing
Structural Testing
Combinational Exhaustive and Pseudo-Exhaustive Testing
Full Exhaustive Testing
Test Styles
Manufacturing Test
The Manufacturing Test Process
Manufacturing Test Load Board
Manufacturing Test Program
Using Automatic Test Equipment
Automatic Test Equipment
ATE Limitations
ATE Cost Considerations
Test and Pin Timing
Tester and Device Pin Timing
Tester Edge Sets
Tester Precision and Accuracy
Manufacturing Test Program Components
The Pieces and Parts of a Test Program
Test Program Optimization
Recommended Reading
Automatic Test Pattern Generation Fundamentals

Introduction to Automatic Test Pattern Generation

Purpose

Introduction to Automated Test Pattern Generation

The Vector Generation Process Flow

The Reasons for ATPG

Why ATPG? Pro and Con Perceptions of ATPG

The Automatic Test Pattern Generation Process

Introduction to ATPG

Introducing the Combinational Stuck-At Fault

Combinational Stuck-At Faults

Combinational Stuck-At Fault Detection

Introducing the Delay Fault

Delay Faults

Delay Fault Detection

Introducing the Current-Based Fault

Current-Based Testing

Current-Based Testing Detection

Testability and Fault Analysis Methods

Why Conduct ATPG Analysis or Testability Analysis? What Types of Testability Analysis Are Available? Fault Effective Circuits

Controllability-Observability Analysis

Circuit Learning

Fault Masking

Causes and Effects of Fault Masking

Fault Masking on Various Fault Models

Stuck Fault Equivalence

Fault Equivalence Optimization

Fault Equivalence Side Effects

Stuck-At ATPG

Fault Selection

Exercising the Fault

Detect Path Sensitization

Transition Delay Fault ATPG

Using ATPG with Transition Delay Faults

Transition Delay Is a Gross Delay Fault

Path Delay Fault ATPG

Path Delay ATPG

Robust Fault Detection

The Path Delay Design Description

Path Enumeration
Current-Based Fault ATPG
Current-Based ATPG Algorithms
Combinational versus Sequential ATPG
multiple Cycle Sequential Test Pattern Generation
Multiple Time Frame Combinational ATPG
Two-Time-Frame ATPG Limitations
Cycle-Based ATPG Limitations
Vector Simulation
Fault Simulation
Simulation for Manufacturing Test
ATPG Vectors
Vector Formats
Vector Compaction and Compression
ATPG-Based Design Rules
The ATPG Tool "NO" Rules List
Exceptions to the Rules
Selecting an ATPG Tool
The Measurables
The ATPG Benchmark Process
ATPG Fundamentals Summary
Establishing an ATPG Methodology
Recommended Reading
Scan Architectures and Techniques
Introduction to Scan-Based Testing
Purpose
The Testing Problem
Scan Testing
Scan Testing Misconceptions
Functional Testing
The Scan Effective Circuit
The Mux-D Style Scan Flip-Flops
The Multiplexed-D Flip-Flop Scan Cell
Perceived Silicon Impact of the Mux-D Scan Flip-Flop
Other Types of Scan Flip-Flops
Mixing Scan Styles
Preferred Mux-D Scan Flip-Flops
Operation Priority of the Multiplexed-D Flip-Flop Scan Cell
The Mux-D Flip-Flop Family
The Scan Shift Register or Scan Chain
The Scan Architecture for Test
The Scan Shift Register (a.k.a The Scan Chain)
Scan Cell Operations
Scan Cell Transfer Functions
Scan Test Sequencing
Scan Test Timing
Safe Scan Shifting
Safe Scan Sampling: Contention-Free Vectors
Contention-Free Vectors
Partial Scan
Scan Testing with Partial-Scan
Sequential ATPG
multiple Scan Chains
Advantages of Multiple Scan Chains
Balanced Scan Chains
The Borrowed Scan Interface
Setting up a Borrowed Scan Interface
The Shared Scan Input Interface
The Shared Scan Output Interface
Clocking, On-Chip Clock Sources, and Scan
On-Chip Clock Sources and Scan Testing
On-Chip Clocks and Being Scan Tested
Scan-Based Design Rules
Scan-Based DFT and Design Rules
The Rules
Stuck-At (DC) Scan Insertion
DC Scan Insertion
Extras
DC Scan Insertion and Multiple Clock Domains
Stuck-At Scan Diagnostics
Implementing Stuck-At Scan Diagnostics
Diagnostic Fault Simulation
Functional Scan-Out
At-Speed Scan (AC) Test Goals
AC Test Goals
Cost Drivers
At-Speed Scan Testing
Uses of At-Speed Scan Testing
At-Speed Scan Sequence
At-Speed Scan versus DC Scan
The At-Speed Scan Architecture
At-Speed Scan Interface
At-Speed "Safe Shifting" Logic
At-Speed Scan Sample Architecture
The At-Speed Scan Interface
At-Speed Scan Shift Interface
At-Speed Scan Sample Interface
multiple Clock and Scan Domain Operation
multiple Timing Domains
Scan Insertion and Clock Skew
multiple Clock Domains, Clock Skew, and Scan Insertion
Multiple Time Domain Scan Insertion
Scan Insertion for At-Speed Scan
Scan Cell Substitution
Scan Control Signal Insertion
Scan Interface Insertion
Other Considerations
Critical Paths for At-Speed Scan
Critical Paths
Critical Path Selection
Path Filtering
False Path Content
Real Critical Paths
Critical Path Scan-Based Diagnostics
Scan-Based Logic BIST
Pseudo-Random Pattern Generation
Signature Analysis
Logic Built-In Self-Test
LFSR Science (A Quick Tutorial)
X-Management
Abasing
Scan Test Fundamentals Summary
Recommended Reading
Memory Test Architectures and Techniques
Introduction to Memory Testing
Purpose
Introduction to Memory Test
Types of Memories
Categorizing Memory Types
Memory Organization
Types of Memory Organization
Chip Assembly Using Reuse Cores
What Is a Core?
Defining Cores
The Core DFT and Test Problem
Built-In DFT
What is Core-Based Design?
Design of a Core-Based Chip
Core-Based Design Fundamentals
Reuse Core Deliverables
Embedded Core Deliverables
Core DFT Issues
Embedded Core-Based Design Test Issues
Development of a Reusable Core
Embedded Core Considerations for DFT
DFT Interface Considerations-Test Signals
Embedded Core Interface Considerations for DFT-Test Signals
Core DFT Interface Concerns-Test Access
Test Access to the Core Interface
DFT Interface Concerns-Test Wrappers
The Test Wrapper as a Signal reduction Element
The Test Wrapper as a Frequency Interface
The Test Wrapper as a Virtual Test Socket
The Registered Isolation Test Wrapper
The Slice Isolation Test Wrapper
The Isolation Test Wrapper-Slice Cell
The Isolation Test Wrapper-Core DFT Interface
Core Test Mode Default Values
Internal versus External Test Quiescence Defaults Application
DFT Interface Wrapper Concerns
Lack of Bidirectional Signals
Test Clock Source Considerations
DFT Interface Concerns-Test Frequency
Embedded Core Interface Concerns for DFT-Test Frequency
Solving the Frequency Problem
Core DFT Development
Internal Parallel Scan
Wrapper Parallel Scan
Embedded Memory BIST
Other DFT Features
Core Test Economics