ASMC 2013 - TABLE OF CONTENTS

These technical proceedings contain copyrighted manuscripts from the 2013 24th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC). Every effort has been made to ensure accuracy. However, IEEE and SEMI cannot be held responsible for errors or omissions. The listings and contents of these proceedings are proprietary and cannot be reproduced in part or in whole without the express written consent of IEEE, SEMI and the author(s).

Session 1 - Advanced Patterning/ Design for Manufacturing

1.1 Cost Effective Application of Advanced Computational Lithography Techniques Using Flexible Mask Optimization
   Gek Soon Chua, Yi Zou, Wei-Long Wang, GLOBALFOUNDRIES; Jianhong Qiu, Taksh Pandey, Stanislas Baron, Sanjay Kapasi, Russell Dover, Xiaolong Zhang, Bo Yan, ASML Brion

1.2 Fast and Accurate Design Based Binning Based on Hierarchical Clustering with Invariant Feature Vectors for BEOL
   Katsuyoshi Miura, Yuki Soga, Koji Nakamae, Osaka University; Kenichi Kadota, Toshiyuki Aritake, Yuichiro Yamazaki, Toshiba Corporation

1.3 Characterization methodology to support process development of advanced patterning structures

1.4 Feasible Industrial Fabrication of Thin Film Transistor based on Randomized Network of Single Walled Carbon Nanotube
   Sayed Alireza Mousavi, Patrizia Lamberti, Vincenzo Tucci, University of Salerno; Veit Wagner, Jacobs University Bremen

1.5 Investigation of Shape Etching on Multi-layer SiO2/Poly-Si for 3D NAND Architecture
   Zusing Yang, Fang-Hao Hsu, Lo Yueh Lin, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen and Chih-Yuan Lu Macronix International Co.

Session 2 - Factory Optimization I

2.1 Designing Product Workflow for Logistics – a Hidden Potential for Cycle Time and Cost Reduction as well as Quality Improvement in High-Tech-Factories
   Sophia Kell, Rainer Lasch, Dresden University of Technology; Dietrich Eberts, Infineon Technologies Dresden

2.2 An Effective Problem Decomposition Method for Scheduling of Diffusion Processes Based on Mixed Integer Linear Programming
Session 3 - 3D/TSV Technology

3.1 Novel Photodefined Polymer-Clad Through-Silicon Via Technology Integrated With End Point Detection Using Optical Emission Spectroscopy
Paragkumar A. Thadesar, Ashish Dembla, Gary S. May, Muhannad S. Bakir, Georgia Institute of Technology; Ja Myung Gu, Sang Jeen Hong, Myongji University

3.2 Challenges in Thin Wafer Handling and Processing
Stephen Olson, Klaus Hummler, Brian Sapp, SEMATECH

3.3 Mechanical Characteristics of Thin Dies/Wafers in Three Dimensional Large-Scale Integrated Systems
Mariappan Murugesan, T. Fukushima, J.C. Bea, K.W. Lee, H. T. Tanaka, M. Koyanagi, Tohoku University

3.4 TSV Density Impact on 3D Power Delivery with High Aspect Ratio TSVs
Huanyu He, James J-Q. Lu, Rensselaer Polytechnic Institute; Zheng Xu, Xiaoxiong Gu, IBM

3.5 Metrology and Inspection Challenges for Manufacturing 3D stacked IC's
Sandip Halder, Karen Stiers, Andy Miller, Ingrid de Wolf, Mireille Maenhoudt, Eric Beyne; IMEC, Stefano Guerrieri, Micron Technology

Session 4 - Factory Optimization II

4.1 Organizational Learning and Capital Productivity in Semiconductor Manufacturing
Charles M. Weber, Jiting Yang, Portland State University

4.2 Eradicating Human Errors during Preventive Maintenance: Understanding the Psychological Reasons We Make Errors and Implementing Proactive Practices to Manage and Reduce Human Errors
Peter Gaboury, Angeline Ottoini, Bruno Spanu, Gerard Chaix, Laurence Philippon, STMicroelectronics
4.3 **Automation: Key to Cycle Time Improvement in Semiconductor Manufacturing** 93
Amit Sonar, Satyajit Shinde, Susanto Teh, GLOBALFOUNDRIES

4.4 **Automated Metrology Recipe Creation** 99
Andrew Haskins, Andre Holfeld, GLOBALFOUNDRIES

4.5 **Deploying an Equipment Health Monitoring Dashboard and Assessing Predictive Maintenance**
James Moyne, Jimmy Iskandar, Parris Hawkins, Applied Materials; Toysha Walker, Micron; David Stark, ISMI; Avi Furest and Bryan Pollard, Intel Corporation

**Session 5 - Interactive Poster Session**

5.1 **The Analysis of Process Queue Time in a Foundry Environment** 111
Michael Alan Retersdorf, Ulf Lederer, GLOBALFOUNDRIES

5.2 **A Bottom-Up Search Technique of Manufacturing Indicators** 115
Jacques Pinaton, STMicroelectronics; Sara Bouzid, Corine Cauvet, Claudia Frydman, LSIS laboratory

5.3 **Cu/Ni Interface Study for Bump Reliability Improvement** 121
Rung-De Wang, Taiwan Semiconductor Manufacturing Company, Ltd.

5.4 **Design-enabled Manufacturing Enablement using Manufacturing Design Request Tracker (MDRT)** 126

5.5 **Die Level Defects Detection in Semiconductor Units** 130
Asaad Said, Nital Patel, Intel Corporation

5.6 **Efficiency in Sealing: A BKM Case Study** 134
Dalia Vernikovsky, Applied Seals North America; Brad Ecker, Seth Urbach, Microchip Technology

5.7 **Equipment Automation Framework with embedded Interface-A** 138
Bert Müller, Jochen Kinauer, AIS Automation Dresden GmbH

5.8 **Glass Substrates for Carrier and Interposer Applications and Associated Metrology Solutions** 142
Aric B. Shorey, John T. Keech, Corning Incorporated

5.9 **Improvement of Lithography Process by Using SMO for 14nm FINFET Application** N/A
Jung Yu Hsieh, Yayi Wei, GLOBALFOUNDRIES

**A Lean Approach to Human Performance** 151
5.10 Michael E. Lombardi, Intel Corp.

5.11 Maintaining Abatement Efficiency while Increasing Utility Efficiency Using the Applied iSYSTM Controller
   Monique McIntosh, Applied Materials

5.12 New Vaporization Sources for H2O2 for Pre-treatment/Cleaning of ALD Deposition Surfaces

5.13 The N2 diluted application in PECVD NF3 in-situ chamber cleaning for PFC reduction

5.14 Overlay Mark Contrast Enhancement for Double Patterning 
   Sohan Singh Mehta, Herrick Matthew, Tsai Huai-Hsuan, Lokesh Subramany, Michael Anderson, Jeon Bumhwan, Yayi Wei, GLOBALFOUNDRIES

5.15 Purging of Front Opening Unified Pod for 450 mm Wafer Manufacturing
   Chun-Yong Khoo, Shih-Cheng Hu, Tze-Yu Huang, Cheng-Wei Yang, National Taipei University of Technology

5.16 Qualification Management and Its Impact on Capacity Optimization
   Mehdi Rowshannahad, Stéphane Daузère-Pérès, Ecole des Mines de Saint-Etienne; Bernard Cassini, Soitec

5.17 Practical aspects of Virtual Metrology and Predictive Maintenance model
   Development and Optimization
   U. Schöpka, Lothar Pfitzner, G. Roeder, A. Mattes, M. Schellenberger, M. Pfeffer, P. Scheibelhofer, ams AG/Graz University of Technology

5.18 A Process to Reduce the Occurrence of Metal Extrusions in Al Interconnects
   Shawn Adderly, IBM Microelectronics

5.19 Rough Film Wafer Sensitivity Improvement using Light Scattering Inspection System
   Chuanyong Huang, Raymond Chu, Gordana Nešković, KLA-Tencor

5.20 Simulations of "Atomistic" Effects in Nanoscale Dopant Profiling
   Petru Andrei, Mohit Mehta, Florida State University; Mark Hagmann, Newpath Research

Session 6 - Yield Enhancement I

6.1 Effective Co-optimization of DFM and Defect Inspection Methods for Fast Yield Ramp
   Yan Pan, Rao Desineni, Jane Lambert, Edward Teoh, Victor Lim, Goh Szu Huat, Thomas
6.2 Use of Performance Path Test to Optimize Yield 206
Jeanne Paulette Bickford, Jinjun Xiong, IBM

6.3 Statistical Correlation of Inline Defect to Sort Test in Semiconductor Manufacturing
Uwe Hessinger, Brett Schafman, Wendy Chan, Toan Nguyen, Shiree Burt, Lattice Semiconductor Corporation

6.4 Heading Towards Big Data: Building A Better Data Warehouse For More Data, More Speed and More Users 220
Raymond Goss, Kousikan Veeramuthuk GLOBALFOUNDRIES

6.5 Case Studies of Fault Isolation for the Global Failing Patterns on SRAM Bitmap caused by the Defects in Peripheral Logic Regions
Jianhua Yin, Jian Yu, Sheng Xie, Dapeng Sun, Yong Ern Ling, GLOBALFOUNDRIES; Zhigang Song, Carl E. Schiller, Genadi Teverskoy, Manuel J. Villalobos, IBM

Session 7 - Advanced Metrology I

7.1 Composition Measurement Of Tri-layer SiGe Stack Using Broadband Spectroscopic Ellipsometry
Michael Anderson, Felipe Tijiwa Birk, Alok Vaid, GLOBALFOUNDRIES; Leander Haensel, Ronny Haupt, Carlos Ygartua, Frank Shu, KLA-Tencor

7.2 MBIR for In-line Doping Metrology of Epitaxial SiGe:B and SiC:P Layers 237
Romain Duru, Delphine LE-CUNFF, Yves Campidelli, D. Barge, STMicroelectronics; Nicolas Laurent, Jonny Hoglund, Semilab

7.3 Full Wafer Nanotopography Analysis on Rough Surfaces Using Stitched White Light Interferometry Images
Dirk Lewke, Martin Schellenberger, Lothar Pfitzner, Fraunhofer Institute of Integrated Systems and Device Technology (IISB); Thomas Fries, Bastian Tröger, Alexander Muehlig, FRT GmbH; Frank Riedel, Stefan Bauer, Hubert Wihr, Siltronic AG

7.4 3D X-Ray Microscopy: A Non-Destructive High Resolution Imaging Technology That Replaces Cross-Sectioning for 3D IC Packaging
Yuri Andrade Sylvester, Luke Hunter, Bruce Johnson, Xradia; Tulip Chou, TSMC

7.5 Leveraging Applied Materials TechEdge PrizmTM for Advanced Lithography Process Control
Paul Llanos, Roger Cornell, Applied Materials

Session 8 - Defect Inspection I

8.1 Optimizing Inspection Recipes by Using Virtual Inspector Virtual Analyzer and
Failure Bitmap
Roma Jang, Dongchul Ihm, Byoungho Lee, Samsung Electronics Co. Ltd; Gangadharan Sivaraman, Chang Ho Lee, Jian Wu, Graham Lynch, George Simon, Poh Boon Yong, KLA-Tencor

8.2 Leveraging Puma DF Wafer Inspection to Characterize Root Cause of Yield Loss on an advanced 32 Nm HKMG SOI Technology Device
Alisa Blauberg, Tom Timberlake, Andrew Stamper, Daniel Jaeger, Mary Jane Brodsky, Renee Mo, IBM Corporation; Gangadharan Sivaraman, Jeff Barnum, Gary Crispo, KLA-Tencor

8.3 Defect Sampling Methodology for Yield Learning During 22nm Process Development
Julie Lee, Chen Xu, Vikas Sachan, Oliver D. Patterson, IBM

8.4 Systematic Edge Inspection for Defect Reduction
Pratik Joshi, R. Van Roijen, J. Coffin, S. Conti, P. Flaitz, J. Eastman, IBM

Session 9 - Advanced Equipment Processes and Materials

9.1 Advanced Process Control for Furnace Systems in Semiconductor Manufacturing
Amit Sonar, Satyajit Shinde, Yulei Sun, GLOBALFOUNDRIES

9.2 Pre-Clean Synergy with Poly CMP Process
Lai Kah Keen, Goh, Wooi Cheang; Chen Yan; Peck, Yan Zheng; Park, Won Gyu; GLOBALFOUNDRIES (Singapore) Pte Ltd

9.3 Novel Process Strategies for Strip over TiN
Li Diao, Vijay Vaniapura, Robert Mueller, Mattson Technology, Inc.

9.4 Methods of Removing Solvent-like Residues from Wafer Backside Bevel
Sheng-Yuan Chang, Cheng-Yi Lung, An Chyi Wei, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen and Chih-Yuan Lu; Macronix International Co., Ltd.

Session 10 - E-Beam Inspection

10.1 Early Detection of Systematic Patterning Problems for a 22nm SOI Technology using E-Beam Hot Spot Inspection
Oliver D. Patterson, Deborah A. Ryan, Mike D. Monkowski, Dominique Nguyen-ngoc, Bradley Morganfeld, IBM; Chung-ham Lee, Chieh-hung Liu, Chi-ming Chen, Shih-tsung Chen, Hermes Macrovision Inc.

10.2 Early Detection of Electrical Defects in Deep Trench Capacitors using Voltage Contrast Inspection
Brian Donovan, Oliver D. Patterson, W. Chang, N. Arnold, B. Messenger, O. Kwon, J. Liu, IBM; Roland Hahn, KLA-Tencor

10.3 E-beam Inspection for Gap Physical Defect Detection in 28nm CMOS Process
Session 11 - APC

11.1 Case of Small-Data Analysis for Ion Implanters in the Era of Big-Data FDC
Keung Hui, Jason Mou, Taiwan Semiconductor Manufacturing Company

11.2 Characterization and Real Time Fault Detection of Vacuum Leaks in Plasma Nitridation Tools
Joseph F. Shepard, Jr., Mark L. Reath, IBM Microelectronics; James K. Wilson, Applied Materials

11.3 Virtual Metrology for Prediction of Etch Depth in a Trench Etch Process
Georg Roeder, Martin Schellenberger, Lothar Pfitzner, Fraunhofer Institute of Integrated Systems and Device Technology (IISB); Sirko Winzer, Stefan Jank, Infineon Technologies

11.4 Application of PCA for Efficient Multivariate FDC of Semiconductor Manufacturing Equipment
Alexis Thieullen, Mustapha Ouladsine, Aix-Marseille University; Jacques Pinaton, STMicroelectronics

Session 12 - Yield Enhancement II

12.1 Defect Reduction by Nitrogen Purge of Wafer Carriers
Raymond Van Roijen, P. Joshi, S. Conti, W. Brennan, P. Findeis, IBM; D. Bailey, PDF Solutions

12.2 Single Wafer Cleaning Lessons in Advanced Node Gate Module Development
David F. Hilscher, Daniel Jaeger, Charlotte DeWan, Maryjane Brodsky, Ryan Rettmann, IBM Semiconductor Research and Development Center

12.3 Hybrid Clean Approach for Post Copper CMP Defect Reduction
Wei-Tsu Tseng, Vamsi Devarapalli, James Steffes, Adam Ticknor, Mahmoud Khojasteh, Praneetha Poloju, Colin Goyette, David Steber, Leo Tai, Steven Molis, Mary Zaitz, Elliott Rill, Surbhi Mittal, Michael Kennett, Laertis Economikos, George Ouimet, Christine Bunke, Connie Truong, Stephan Grunow, Michael Chudzik, IBM

Session 13 - Advanced Metrology II
13.1 Scatterometry-based On-product Focus Measurement and Monitoring 352
Timothy A. Brunner, Cheuk W. Wong, Pawan Rawat, IBM SRDC; Paul Hinnen, Vivien Wang, Hossein Mardanpour, Jan Beltman, Erica Rottenkolber, Christian Leewis, ASML

13.2 Advanced Litho-Cluster Control via Integrated In-Chip Metrology 360
Kaustuve Bhattacharyya, Henk-Jan H. Smilde, Arie den Boef, Andreas Fuchs, Steffen Meyer, ASML Netherlands B.V.; Chih-Ming Ke, Guo-Tsai Huang, Kai-Hsiung Chen, Taiwan Semiconductor Manufacturing Company, Ltd.

13.3 Automated Transmission Electron Microscopy for Defect Review and Metrology of Si Devices 366
Michael Strauss and Mark Williamson, FEI Company

Session 14 - Defect Inspection II

14.1 GaN-On-Si Process Defect Detection and Analysis for HB-LED’s and Power Devices 371
Sandip Haider, Karen Stiers, Prem Kumar Kandaswamy, Maarten Rosmeulen, Laureen Carbonell, Yoga Saripalli, Haris Osman, Erik Rosseel, imec; Antonio Mani, Srinivas Vedula, Marco Polli, KLA-Tencor

14.2 Detecting Yield Limiting SiGe Defects for 28nm Ramping 375
Elston Chen, Wen Pang Lin, Garry Chen, P Y Chiang, White Pai, United Microelectronics Corporation; Sam Chen, Mahatma Lin, Frank Jin, Eros Huang, Harvey Cheng, Tetsuya Yamamoto, KLA-Tencor Corporation

14.3 On the Generation and Elimination of Lonely Poly-Silicon Crater-Defects and their Impacts on Gate Oxide Integrity (GOI) in Dual-Gate Technology 378
Lieyi Sheng, Paul Porath, Eddie Glines, ON Semiconductor

14.4 In-situ Detection of Photoresist Failures 382
Farhad Mirian, Thomas Bitzer, Infineon Technologies AG

Session 15 - Advanced Equipment Processes and Materials

15.1 Recent Advances in Memory Technology 386
Dick James, Chipworks Inc.

15.2 Integrating Spin-Torque-Transfer Magnetic Memory in a 65 nm Low Power CMOS Technology 396
Douglas Coolbaugh, Michael Liehr, Michelle Pautler, College of Nanoscale Science and Engineering; Rajiv Ranjan, Ebi Abedifard, Avalanche Technology

15.3 Improving Electric Behavior and Simplifying Production of Si-Based Diodes by Using Thermal Laser Separation 400
Matthias Koitzsch, Dirk Lewke, Martin Schellenberger, Lothar Pfitzner, Heiner Ryssel, Fraunhofer Institute of Integrated Systems and Device Technology (IISB); Robert Kolb, Robert Bosch GmbH; Hans-Ulrich Zühlke, Jenoptik Automatisierungstechnik GmbH
Contamination Control and Pilot Manufacturing of Commercial Grade Carbon Nanotube Colloidal Formulations

Billy Smith, Thomas Kocab, Rahul Sen, David A. Roberts, Nantero Inc.

2013 SEMI Advanced Semiconductor Manufacturing Conference