LOGIC NON-VOLATILE MEMORY
The NVM Solutions from eMemory

Charles Ching-Hsiang Hsu
Chairman of eMemory Technology, Inc., Taiwan

Yuan-Tai Lin
Chief Technology Officer of eMemory Technology, Inc., Taiwan

Evans Ching-Sung Yang
Vice President of eMemory Technology, Inc., Taiwan

Rick Shih-Jye Shen
President of eMemory Technology, Inc., Taiwan
LOGIC NON-VOLALITILE MEMORY
The NVM Solutions from eMemory

Contents

Foreword vi
Preface vii
Acknowledgements xv

Contents xxiii
List of Figures xxvii
List of Tables xxxiii

Chapter 1 Introduction

Section 1.1 What Are Logic NVMs 3
Section 1.2 When to Use Logic NVM 5
Section 1.3 Why Use Logic NVM 6
Section 1.4 Which Logic NVM is Better to Use 8
Section 1.5 Where to Get the Logic NVM Platform 9
Section 1.6 How to Use Logic NVM 11
References 13

Chapter 2 One Time Programmable (OTP) Memory

Section 2.1 OTP (NeoBit) Cell 17
2.1.1 Cell Structure, 17
2.1.2 Why pMOST, 18
2.1.3 Programming Mechanism, 20
2.1.4 Erase Mechanism, 22
2.1.5 Read Operation, 22
2.1.6 Data Retention, 24
2.1.7 Program Disturb, 27
2.1.8 Read Disturb, 27

Section 2.2 Process Integration 28
2.2.1 Gate Oxide Formation, 29
2.2.2 Contact Etch Stop Layer Capacitor Deposition, 29
2.2.3 BEOL Tungsten CMP and High-Density-Plasma Oxide Deposition, 29
2.2.4 Ultraviolet Transparent Passivation Layer Deposition, 30
Contents

3.1.5 Array Architecture, 108
3.1.6 Array Disturb, 109
3.1.7 Endurance, 112
3.1.8 Data Retention, 113
3.1.9 Operation Window, 116
3.1.10 Ramping CL PGM Scheme, 118

Section 3.2

Process Integration
3.2.1 Isolation, 129
3.2.2 Deep n-Well (DNW) Process, 130
3.2.3 ONO Film Formation, 131
3.2.4 Poly Gate Formation, 133
3.2.5 Reverse ONO Etch, 134

Section 3.3

Reliability
3.3.1 Gate Oxide Reliability – Time-Dependent Dielectric Breakdown (TDDB), 135
3.3.2 Endurance, 138
3.3.3 High Temperature Data Retention – Ea Value Extrapolation, 139

Section 3.4

Design
3.4.1 Read/Write Cell Bias Condition, 143
  3.4.1.1 Read Operation Cell Bias, 145
  3.4.1.2 Write Operation Cell Bias, 147
3.4.2 Block Diagram of NeoFlash IP, 148
3.4.3 Decoding System Introduction, 149
3.4.4 Sense Amplifier, 151
3.4.5 PGM/ERS with PV/EV Scheme, 152
3.4.6 HV System Introduction, 154
3.4.7 Charge Pumping Circuit, 155
3.4.8 Test Mode Function Introduction, 158

Section 3.5

Test Flow and Characterization
3.5.1 Test Flow, 161
3.5.2 Characterization, 166

Section 3.6

Qualification

Section 3.7

Applications

Section 3.8

IP Specifications

Section 3.9

Flash to ROM Conversion

References

Chapter 4 EEPROM

Section 4.1

Device
4.1.1 EEPROM (Electrically Erasable Programmable Read Only Memory), 185
4.1.2 Nitride Storage Solutions, 190
  4.1.2.1 Toshiba, 190
  4.1.2.2 Fujitsu, 191
  4.1.2.3 IBM, 193
  4.1.2.4 Tower Semiconductor (S-Flash), 195
  4.1.2.5 NTHU (SAN), 197
  4.1.2.6 Challenges for Nitride Storage Solutions, 200
4.1.3 Floating Gate Solutions, 203
  4.1.3.1 Toshiba, 203
  4.1.3.2 IBM, 204
  4.1.3.3 Bell Labs, 206
  4.1.3.4 Impinj, 208
  4.1.3.5 Tower Semiconductor, 210
  4.1.3.6 Yield Microelectronics Corp. (YMC), 211
  4.1.3.7 Challenges of Floating Gate Solutions, 215
4.1.4 NeoEE Technology, 217
  4.1.4.1 Device Operation, 218
  4.1.4.2 Device Characterization and Reliability, 221
  4.1.4.3 BYTE-Erasable EEPROM Architecture, 224
Section 4.2 Process Integration 226
  4.2.1 HV Devices, Rules & Reliability, 226
  4.2.2 Logic Circuit Manufacturing Process Derivatives, 230
  4.2.3 Challenges at Advanced Technology Nodes, 231
Section 4.3 NeoEE Design Introduction 232
  4.3.1 NeoEE Design Challenges, 232
  4.3.2 NeoEE Array Architecture, 234
  4.3.3 NeoEE READ Design, 236
  4.3.4 NeoEE HV Design, 237
    4.3.4.1 NeoEE HV Power Generation, 238
    4.3.4.2 NeoEE HV Power Delivery, 240
  4.3.5 NeoEE Test Mode Design, 247
Section 4.4 Characterization and Reliability 248
Section 4.5 Applications 249
Section 4.6 IP Specifications 249
References 251

Chapter 5 Non-Volatile Memory IP Foundry

Section 5.1 IP Developing Flow 255
  5.1.1 Marketing Survey, 255
  5.1.2 Process Development and Qualification, 256
  5.1.3 IP Design and Production, 257
Section 5.2 IP Design and Layout Flow 259
  5.2.1 Project Feasibility Assessment, 259
  5.2.2 Project Planning, 259
<table>
<thead>
<tr>
<th>Section 5.3</th>
<th>IP Service Flow</th>
<th>262</th>
</tr>
</thead>
<tbody>
<tr>
<td>Section 5.4</td>
<td>IP Deliverables and Security</td>
<td>264</td>
</tr>
<tr>
<td>5.4.1 IP Design Kits, 264</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.4.2 IP Tape-Out Kits, 265</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Section 5.5</td>
<td>Intelligent System for IP Production</td>
<td>266</td>
</tr>
<tr>
<td>Index</td>
<td></td>
<td>269</td>
</tr>
</tbody>
</table>