WA3

Ceramic & LTCC Packaging

Chairs: Dan Krueger, Honeywell FM&T; Ken Peterson, Sandia National Lab.

0617 -- Comparison of Silver vs. Gold Systems in High-Q FTTF LTCC Inductors
Matthew Clewell, Kansas State University (William B Kuhn)

0622 -- Evaluation of Exothermic Reactions in Cofired Platinum /Alumina Microsystems
Kinzy Jones, Florida International University (Ali Karbasi)

0628 -- Radiation Mechanisms and Electromagnetic Interference in Ceramic Electronic Packages
Jerry Aguirre, Kyocera America Inc (Marcos Vargas)

WA4

Wirebonding, Stud Bumping & Substrate Materials 2

Chairs: Bernd Appelt, ASE US; Mike Ferrara, RF Micro Devices

In this session new observations in wire bond assembly will be discussed followed materials and process effects on substrates and assembly.

0638 -- Copper Wire Bonding: R&D to High Volume Manufacturing
Bob Chylak, Kulicke and Soffa Industries, Inc. (Horst Clauberg, John Foley, Ivy Qin)

0650 -- IC Bond Pad "Ripple Effect" Investigation
Stevan Hunter, ON Semiconductor (Darin Hornberger, Lance Rubio, Lynda Pierson)

0657 -- How to Deal with Resonances in Wirebonding
Dr Josef Sedlmair, F&K Delvotec Bondtechnik GmbH

0665 -- Response of Long Sculpted Wire Bonds to Vibrational Excitation
Thomas F. Marinis, Charles Stark Draper Laboratory (Joseph W. Soucy)

0677 -- A Process For Treating Woven Glass Cloth
Dylan Boday, IBM Corp (Joe Kuczynski, Michael Haag, Johannes Windeln, Michael Waal)
High Performance Interconnect & Boards
Chairs: Julie Adams, Suntron Corp., Steven Davidson, Northrop Grumman

Increased wiring density, performance, reliability issues, and migration to lead free processes impart numerous challenges to the design and fabrication of high performance interconnects and PCBs. Issues related to reliability and performance, from the woven glass cloth to embedded components, drive board design and assembly considerations.

0683 -- Novel ESD Protection Scheme for Testing High Voltage LDMOS
Kaushal Kannan, The University of Alabama, Tuscaloosa (Sukeshwar Kannan, Bruce C. Kim, Friedrich Taenzler, Richard Antley, Ken Moushegian)

0687 -- Making New from Old
Nick Renaud-Bezot, AT&S (Mark Beesley)

0694 -- Photostabilization of i-line Photoresist and ARC Layer
Zeliha Yilmaz, Tubitak Bilgem (Murat Pak, Sema Amrah Ayalas, Aylin Ersoy)

0702 -- 2D Critical Dimension Optimization of Sub-micron Patterns using an Experimental Methodology
Murat Pak, TUBITAK (Aylin Ersoy, Zeliha Yilmaz)

European Perspective 2
Chairs: Ivan Ndip, Fraunhofer IZM; Gabriel Pares, CEA LETI

In this session, reliable methods for measuring wafer stiffness, for electrolytic deposition of solder bumps, heat dissipation and chip stacking are presented. Innovative printing processes are also discussed.

0710 -- Ultra thin chips stacking on tsv silicon interposer using back-to-face technology
Gabriel PARES, CEA-Leti (F. Schnegg, A. Attard, D. Cruau, F. De Crecy, A. Nahari, R. Anciant, G. Klug, H. Luesebrink, K. Martinschitz, C. Karoui, G. Simon)

0720 -- Method to measure wafer stiffness in Fan-Out Wafer Level Package
Jorge Manuel Soares Teixeira, NANIUM, S.A.

0729 -- Electrolytic Deposition of Fine Pitch Sn/Cu Solder Bumps for Flip Chip Packaging
Stephen Kenny, Atotech Germany (Kai Matejat, Frank Hilbert, Sven Lamprecht)

0735 -- Stacking aspects in the view of scaling
Joeri De Vos, IMEC (Kenneth June Rebibis, Eric Beyne)

0741 -- Aerosol-Jet Printing for Functionalization of Prototyping Materials for Electronic Applications
Johannes Hoerber, University of Erlangen-Nuremberg, Institute for Factory Automation and Production Systems (Christian Goth, Joerg Franke)

0749 -- Formulation of percolating thermal underfills by hierarchical self-assembly of micro- and nanoparticles by centrifugal forces and capillary-bridging
Thomas Brunschwiler, IBM Research – Zurich (Gerd Schlottig, Songbo Ni, Yu Liu, Javier V. Goicochea, Jonas Zurcher, Heiko Wolf)
WP1
Glass Interposers
Chairs: Venky Sundaram, Georgia Tech; Ravi Shenoy, Qualcomm

This session focuses on glass interposer technologies and applications in 2.5D and 3D packaging as a lower cost and lower loss alternative to silicon interposers. Papers will discuss different issues related to design, thin glass wafers and panels, fine pitch through via formation and metallization in glass, electrical performance benefits and reliability of vias in glass, and 2.5D and 3D applications for glass interposers.

0760 -- Glass Wafers as support carriers for wafer thinning processes
Aric Shorey, Corning, Inc (Windsor Thomas)

0765 -- Development of Through Glass Vias (TGV) for 3D-IC Integration
Aric Shorey, Corning, Incorporated (Windsor Thomas, Scott Pollard)

0770 -- Characterization of Interconnects and RF Components on Glass Interposers
Dr. Ivan Ndip, Fraunhofer IZM (Michael Toepper, Kai Loebbicke, Abdurrahman Oez, Stephan Guttowski, Herbert Reichl, Klaus-Dieter Lang)

0781 -- Cost Effective 3D Glass Microfabrication for Advanced Packaging Applications
Jeb H Flemming, 3D Glass Solutions (Kevin Dunn, Carrie Schmidt, James Gouker, Roger Cook)

0785 -- Formation of Through-Glass-Via (TGV) by Photo-Chemical Etching with High Selectivity
Zingway Pei, Industrial Technology Research Institute (ITRI) (Jui-Po Sun, Hsin-Chen Lai, Pei-Jer Tzeng, Cha-Hsin Lin, Tzu-Kun Ku, Ming-Jer Kao)

0793 -- A wafer-level system integration technology incorporates heterogeneous devices
Hiroshi Yamada, Toshiba Corporation, Corporate R&D Center, Electron Devices Laboratory (Yutaka Onozuka, Atsuko Iida, Kazuhiko Itaya, Hideyuki Funaki)

WP2
Package Reliability Testing
Chairs: Adam Schubring, Kyocera America; Akhlaq Rahman, Thin Film Technology Corp.

This session focuses on several reliability characterization techniques and testing results on electronic package. Discussions will vary from environmental effects to different material effects as well as mechanical stress on package. Evolution of different reliability test techniques along with test standards will also be discussed.

0801 -- Isothermal Aging Effects on the Thermal Reliability Performance of Lead-Free Solder Joints
Zhou Hai, Auburn University (Jiawei Zhang, Sivasubramanian Thirugnanasambandam, John L. Evans, M. J. Bozack)

0809 -- Thermal Characterization and Simulation of a fcBGA-H device
Eric Ouyang, StatsChipPAC (Jimmy He, MyoungSu Chae, SeonMo Gu, YongHyuk Jeong, Kyungmoon Kim, Gwang Kim, Billy Ahn)

0818 -- Mechanical Stress Analysis and Evaluation of Hybrid Land Grid Array Attached Large Form Factor Organic Modules
Ying Yu, IBM Corporation (John Torok)
0825 -- Package Reliability Drop Shock and Temperature Cycling Testing Evolution, Challenges, and Trends
Michael Ferrara, RF Micro Devices, Inc.

0829 -- Superior Drop Test Performance of BGA Assembly Using SAC105Ti Solder Sphere
Ning-Cheng Lee, Indium Corporation (Weiping Liu, Indium Corporation and Simin Bagheri, Polina Snugovesky, Jason Bragg, Russell Brush, and Blake Harper, Celestica International Inc.)

0844 -- Solution for HVM TSV Etch Process
Rajiv Roy, Rudolph Technologies, Inc. (Matt Wilson, Product Manager)

WP3
Thermal Management
Chairs: Tom Tarter, Package Science Services, Bernie Siegal, Thermal Engineering Associates

Heat dissipated by electronic components, boards and systems has to be appropriately and timely dissipated to allow and ensure for expected operation and reliability of electronic equipment. In this session, topics presented range from validation procedures and all the way to the introduction of novel cooling techniques of various components and systems from the world of micro-electronics."

0848 -- Accurate prediction of thermal resistance of fet by detailed modeling of heat generation and backend stackup
Qun Wan, RF Micro Devices (Don Willis, Daniel Jin)

0857 -- Design Optimization of Micro-channel Heat Exchanger embedded in LTCC
Aparna Aravelli, University of Miami, FL (Singiresu S Rao, Hari K Adluru)

0866 -- Thermal Power of Mobile Application Processor
Heung Kyu (Henri) Kwon, Samsung Electronics Co. (Jae Choon Kim, Jichhul Kim, Eun Seok Cho)

0873 -- Stacked Chip Thermal Model Validation using Thermal Test Chips
Thomas Tarter, Package Science Services LLC (Bernie Siegal, Thermal Engineering Associates, President)

0882 -- Influence of thermal ageing on Void Content and shear strength for selected lead free Die-Attach
Kenny C. Otiaba, University of Greenwich (N. Raju, R.S. Bhatti, S. Mallik, P. K. Bernasko)

WP4
Flip Chip & Wafer Bumping
Chairs: Lyndon Larson, Dow Corning; Ron Jensen, Honeywell International

The continuing trend toward higher interconnect density, smaller bump geometries, and new lead-free materials presents challenges and reliability concerns for wafer bumping and flip chip assembly processes. This session highlights new developments that address electromigration and other metallization challenges as well as new materials for these applications.

0891 -- Electromigration Performance of Flip-Chips with Lead-Free Solder Bumps between 30 μm and 60 μm Diameter
Rainer Dohle, Micro Systems Engineering GmbH (Andreas Wirth, Joerg Gossler; Stefan Haerter, Joerg Franke, University of Erlangen-Nuremberg (FAPS); Marek Gorywoda, University of Applied Sciences Hof)
WP5
Printed Electronics & Additive Manufacturing
Chairs: John Bolger, US Department of Defense; Andy Tseng, ASE US

This session will cover a variety of topics of interest, from processing schemes for complex structures to characterization of novel materials.

0935 -- Development of Silver Nanoparticle Ink for Printed Electronics
Yiliang Wu, Xerox Research Centre of Canada (Ping Liu, Tony Wigglesworth)

0940 -- High yield embedding of 30um thin chips in a flexible PCB using a photopatternable polyimide based Ultra-Thin Chip Package (UTCP)
Tom Sterken, IMEC-UGent/CMST (Maaike Op de Beeck, Filip Vermeiren, Tom Torfs, Liang Wang, Swarnakamal Priyabadi, Kristof Dhaenens, Dieter Cuypers, Jan Vanfleteren)

0946 -- Additive Manufacturing of Fine Lines and Embedded Electronics for use in Chip Packaging and Microelectronic Systems
Scott Lauer, Advantech US, Inc (Pierluigi Benci, PhD of Compunetix; John Mazurowski, MS of the Penn State Electro-Optics Center; Whit Little, MBA of Advantech US, Inc.)

0949 -- Rediscovering Multilayer Rigid-Flex with Z-interconnect Technology
Rabindra Das, Endicott Interconnect Technologies, Inc. (Frank D. Egito, John M. Lauffer, and Voya R. Markovich)

0955 -- Development of Printed Power Packaging for a High Voltage SiC Module
Douglas C Hopkins, NC State University (Haotao KE)

0961 -- Heterogeneous Process Development for Electronic Device Packaging with Direct Printed Additive Manufacturing
Ricardo Rodriguez, University of Texas, El Paso (Xudong Chen, nScrypt, Kenneth Church Ph.D., UTEP)

WP6
Japan Perspective 2
Chairs: Bill Ishii, Torrey Hills Technologies; Kishio Yokouchi, Fujitsu Interconnect Technologies

This session focuses on various 2.5D / 3D, interposer, and material technologies, as well as design developments in Japan for advanced packaging architectures.

0967 -- Study of warpage and mechanical stress of 2.5D package interposers during chip and interposer mount process
Takashi Hisada, IBM Japan, Ltd. (Yasuharu Yamada, Junko Asai, Toyohiro Aoki)
0975 -- Handling technology for 0.075-square mm powder IC chip  
Hideyuki Noda, Hitachi, Ltd., Central Research Laboratory

0984 -- Full Integration and Electrical Characterization of 3D Silicon Interposer Demonstrator incorporating high density TSVs and interconnects  
Ken Miyairi, SHINKO ELECTRIC INDUSTRIES CO., LTD. (Masahiro Sunohara, Jean Charbonnier, Myriam Assous, Jean-Philippe Bally, Robert Cuchet, Helene Feldis, Gilles Simon and Mitsutoshi Higashi)

0991 -- New Build-up Insulation Material Based on Cyclo-Olefin Polymer for High Performance IC Packages  
Yohei Tateishi, Zeon Corporation (Makoto Fujimura, Toshihiko Jimbo, Takashi Iga)

0998 -- Scallop Free Si Etching and Low Cost Integration Technologies for 2.5D Si Interposer  
Yasuhiro Morikawa, ULVAC, Inc. (Takahide Murayama, Toshiyuki Sakuishi, Manabu Yoshii and Koukou Suu)

1001 -- Thermomechanical Design for Fine Pitch 3D-IC Packages  
Akihiro Horibe, ASET (Sayuri Kohara, Kuniaki Sueoka, Keiji Matsumoto, Yasumitsu Orii, Fumiaki Yamada)

1010 -- Thinner and Miniaturization Embedded Device Package, MCeP, for PoP and Module Application  
Kouichi Tanaka, Shinko Electric Industries Co., LTD. (Nobuyuki Kurashima, Hajime Iizuka, Kiyoshi Ooi, Yoshihiro Machida, Satoshi Shiraki, Tetsuya Koyama)

**Thursday, September 13, 2012**  
**Afternoon Sessions: 1:00pm-4:15pm**

**THP1**  
**3D Thermal/Mechanical**  
**Chairs: Robert Darveaux, Amkor; Alex Bailey, Northrop Grumman**

*This session addresses a variety of critical topics in 3D thermal / mechanical engineering for both portable product and infrastructure applications. New insights into thermal stress analysis, solder joint ductility, copper pillar electromigration, and PoP warpage will be gained.*

1018 -- Electromigration Performance of Fine Pitch Copper Pillar Interconnections  
Ahmer Syed, Amkor Technology, Inc. (Christopher J. Berry, Karthikeyan Dhandapani, Patrick Thompson, Seung-Hyun Chae)

1026 -- Modeling in the Cloud: Web Hosted CPI Modeling for Fabless Design Houses and OSATs  
Method for Mechanical Stress Simulation Across the Chip & Package Domains in 3D IC's  
Mark Nakamoto, Qualcomm (Karthikeyan Dhandapani, Wei Zhao, Ahmer Syed, Wei Lin, Riko Radojcic)

1034 -- PoP package warpage contributors' characterization and impact analysis  
Shengmin Wen, Amkor Technology Inc (Wei Lin, Akito Yoshida)

1038 -- Thermal Stress and Creep Strain Analyses of a 3D IC Integration SiP with Passive Interposer for Network System Application  
John H Lau, ITRI (Sheng-Tsai Wu, John H. Lau*, Heng-Chieh Chien, and Ra-Min Tain, L. Li, P. Su, J. Xue, M. Brillhart)

1046 -- Solder Joint Ductility  
Robert Darveaux, Amkor (Michael Johnson)
THP2

Microwave and RF Applications
Chairs: Jeremy Rodgers, Department of Defense; Christopher Pan, Qualcomm

The RF and Microwave Application section has an array of papers that introduces new interconnect materials, and design and manufacturing techniques for applications at PCB and package levels to meeting the rising challenges in the fields of RF, Microwave, and high data rate digital communication.

1057 -- 3D Electromagnetic Modeling of Through Silicon Vias and Interposers in Electronic Packaging
Darryl Kostka, CST of America (Antonio Ciccomancini Scogna)

1068 -- A Practical Approach to Analyze Copper Surface Roughness Effects with Applications to Stripline Structures
Xichen Guo, University of Houston (Ji Chen, David Jackson, University of Houston; Marina Y. Koledintseva†, James Drewniak, EMC Laboratory, Christopher Pan, FutureWei Technologies)

1073 -- Influence of Different Packaging and Footprint Technique for Microwave Absorptive Bessel Filter's™ Performance
Akhiq Rahman, Thin Film Technology Corporation

1078 -- Qualification of Polyimide Based Coverlays for 900 MHz and 2.40 GHz Microstrip Antenna Applications
Deepukumar Nair, DuPont (Glenn E Oliver, James Parisi)

1081 -- Virtual Ground Fence: A Simple Method for Protection against High Frequency Simultaneous Switching Noise
Jesse Bowman, San Diego State University (A. Ege Engin)

THP3

Automotive, Industrial & Harsh Environment Electronics Applications
Chairs: Larry Zawicki, Honeywell FM&T; Kevin McGrath, Northrop Grumman

This session will provide insight into the challenges related to high power and harsh environmental requirements driving the automotive, industrial and other areas where novel materials and processes are being pursued.

1085 -- Dicing Development for low-k Copper Wafers using Nickel-Palladium-Gold Bond Pads for Automotive Application
Tu Anh Tran, Freescale Semiconductor (Varughese Mathew, Wen Shi Koh, K. Y. Yow, Y. K. Au)

1097 -- Characterization of Over Pad Metallization (OPM) for high temperature reliability
Varughese Mathew, Freescale Semiconductor, Inc. (Tu Anh Tran)

1105 -- Packaging of High Frequency, High Temperature Silicon Carbide (SiC) Multichip Power Module (MCPM) Bi-Directional Battery Chargers for Next Generation Hybrid Electric Vehicles

1116 -- Thin-film High Voltage Capacitors for Hybrid Electric Vehicle Inverter Applications
THP4

Think Thin: Thin IC Packaging For Mobile Devices
Chairs: Steve Bezuk, Qualcomm; Rich Rice, ASE US

Form factor is now a critical selling point for mobile and handheld devices in this day of exploding consumer demand, while the functionality of these devices continues to escalate. IC companies are now pressured more than ever to bring forth thinner packages which combine more functions than ever before. The objective of the "Think Thin" session will be to explore new and alternative technologies that enable packaging to meet the form factor requirements for today, as well as for the future, and will explore the technical issues and challenges that must be overcome.

1131 -- Novel Ultra-Compact Quad-Band System-in-Package (SiP) Module with IC Embedded in Substrate Based on SESUB Technology
Volodymyr Sieroshtan, EPCOS AG (TDK-EPC) (Georgiy Sevskiy, Petro Komakha, Oleg Aleksieiev, Andriy Burygin, Oleg Chayka, Oleksandr Ruban, Mykola Shevelov, Kozo Kato, Akio Horibe, Hideaki Fujioka, Klaus Ruffing, Patric Heide, Martin Vossiek)

1135 -- Going Thin - Potential Challenges Faced By The Industry
Sachin Deo, Micron Technology

1137 -- Fine Pitch Copper Interconnects for Next Generation Package-on-Package (PoP)
Ilyas Mohammed, Invensas, Inc.

1143 -- Embedded Die Substrates for Power Applications
Bernd K Appelt, ASE Group (Bruce Su, Uno Yen, Dora Lee, Kay Essig)

1149 -- Thin Substrates Bursting into the Market
Bernd K Appelt, ASE Group (Bruce Su, Dora Lee, Kidd Lee and Uno Yen)

1155 -- Pushing the 3rd Dimension - Floppy Wafers, Die and Packages? Stress Induced Chip Package Interactions on Thin Mobile Devices
Mark Nakamoto, Qualcomm (Riko Radojcic Wei Zhao)

1162 -- Thin PoP : Warpage control for Thinner PoP package in mobile applications
Yuka Tamadate, Shinko Electric Industries Co., LTD., Seiji Sato, Hitomi Imai, Kota Takeda, Takeshi Meguro and Takashi Ozawa

THP5

Packaging for Light and MEMS
Chairs: John Mazurowski, Penn State Electro Optics Center; Iris Labadie, Kyocera America

New lighting devices and MEMS are changing the industry. High brightness LEDs are overtaking all other device types for illumination applications. In this session, various types of LED, MEMS & sensor devices will be introduced. Materials, fabrication processes, evaluations, and reliabilities for the devices will also be discussed.

1169 -- Highly Flexible Die Attach Adhesives for MEMS Microphone Packages
Dr. Tobias Koeniger, DELO Industrial Adhesives
1178 -- **A Low Firing Temperature Copper Conductor for use on an Aluminum Metal Compatible Dielectric in LED Thermal Substrate Applications**

Samson Shahbazi, Heraeus Precious Metals North America Conshohocken LLC (Steve Grabey, and Ryan Persons)

1185 -- **Hardware Design for Multiple Gas Detection System Using Zeolite Coated with Nile Red**

Son Nguyen, Temple University (Z. Joan Delalic, David M. Kargbo, Joel B. Sheffield)

1191 -- **Development of Synergistic opto-electronic sensing platform based on zinc oxide semiconducting nanopackage**

Anurag Gupta, The University of Alabama-Tuscaloosa (Mitchell Spryn, Sukeshwar Kannan, Bruce Kim, Eugene Edwards, Christina Brantley, Paul Ruffin)

1197 -- **ACES characterization of damping in micro-beam resonators**

Jason Parker, Worcester Polytechnic Institute (Xiuping Chen, Vu Nguyen, Ryszard Pryputniewicz)

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**THP6**

**Taiwan Perspective**

*Chairs: Rajen Chanchani, Consultant; Sam Gu, Qualcomm*

This session focuses on recent advanced package technology progress in Taiwan including 2.5D (large Si interposer) demonstration, electrical characterization of TSV, pre-mold substrate and board level optical interconnect.

1209 -- **Large Size Silicon Interposer and 3D IC Integration for System-in-Packaging (SiP)**

John H. Lau, ITRI (John Lau, Pei-Jer Tzeng, Chau-Jie Zhan, Ching-Kuan Lee, and Ming-Ji Dai, Li Li, Peng Su, Jie Xue, and Mark Buillhart)

1215 -- **GHz High Frequency TSV for 2.5D IC Packaging**

Chi-Han Chen, Advanced Semiconductor Engineering (ASE), Inc. (Chang-Ying Hung, Pao-Nan Lee, Meng-Jen Wang, Chih-Pin Hung, Ho-Ming Tong, ASE, Inc.; Kuan-Chung Lu, Tzyy-Sheng Horng, National Sun Yat-Sen University)

1221 -- **Electrical Performance of Through-Silicon Vias (TSVs) for High-Frequency 3D IC Integration Applications**


1229 -- **Embossed Laminate Optical Layers On Printed Circuit Boards**

Jonas Tsai, University of California Irvine (G.P. Li, Mark Bachman)