<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Authors/Institutions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Keynotes</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Smart Systems for Internet of Things</td>
<td>Benedetto Vigna</td>
</tr>
<tr>
<td></td>
<td>Creating a Sustainable Information and Communication Infrastructure</td>
<td>Massoud Pedram</td>
</tr>
<tr>
<td><strong>2.2 Acceleration and Verification of ESL and Analog Systems</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Moderators: Alper Sen - Bogazici University, TR; Daniel Grosse - University of Bremen, DE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optimized Out-of-Order Parallel Discrete Event Simulation Using Predictions</td>
<td>Weiwei Chen and Rainer Doemer</td>
</tr>
<tr>
<td></td>
<td>Parallel Programming with SystemC for Loosely Timed Models: A Non-Intrusive Approach</td>
<td>Matthieu Moy</td>
</tr>
<tr>
<td></td>
<td>Accuracy vs Speed Tradeoffs in the Estimation of Fixed-Point Errors on Linear Time-Invariant Systems</td>
<td>David Novo, Sara El Alaoui and Paolo Ienne</td>
</tr>
<tr>
<td></td>
<td>Runtime Verification of Nonlinear Analog Circuits Using Incremental Time-Augmented RRT Algorithm</td>
<td>Seyed Nematollah Ahmadyan, Jayanand Asok Kumar and Shobha Vasudevan</td>
</tr>
<tr>
<td></td>
<td>An Automated Parallel Simulation Flow for Heterogeneous Embedded Systems</td>
<td>Seyed Hosein Attarzadeh Niaki and Ingo Sander</td>
</tr>
<tr>
<td></td>
<td>Mutation Analysis with Coverage Discounting</td>
<td>Peter Lisherness, Nicole Lesperance and Kwang-Ting (Tim) Cheng</td>
</tr>
<tr>
<td></td>
<td>Scalable Fault Localization for SystemC TLM Designs</td>
<td>Hoang M. Le, Daniel Grosse and Rolf Drechsler</td>
</tr>
<tr>
<td><strong>2.3 Energy Optimization in Multi-core Systems</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Moderators: Thidapat Chantem - Utah State University, US; William Fomaciari - Politecnico di Milano, IT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cherry-Picking: Exploiting Process Variations in Dark-Silicon Homogeneous Chip Multi-Processors</td>
<td>Bharathwaj Raghunathan, Yatish Turakhia, Siddharth Garg and Diana Marculescu</td>
</tr>
</tbody>
</table>
Energy Optimization with Worst-Case Deadline Guarantee for Pipelined Multiprocessor Systems .................................................. 45
Gang Chen, Kai Huang, Christian Buckl and Alois Knoll

Self-Adaptive Hybrid Dynamic Power Management for Many-Core Systems .......................................................... 51
Muhammad Shafique, Benjamin Vogel and Jörg Henkel

SmartCap: User Experience-Oriented Power Adaptation for Smartphone’s Application Processor .......................................................... 57
Xueliang Li, Guihai Yan, Yinhe Han and Xiaowei Li

Runtime Power Estimation of Mobile AMOLED Displays .......................................................... 61
Dongwon Kim, Wonwoo Jung and Hojung Cha

2.4 Memory and Cache Architectures
Moderators: Georgi Gaydadjiev - Chalmers University of Technology, SE; Todd Austin - Michigan University Ann Arbor, US

AVICA: An Access-time Variation Insensitive L1 Cache Architecture .......................................................... 65
Seokin Hong and Soontae Kim

Dual-addressing Memory Architecture for Two-dimensional Memory Access Patterns .................................................. 71
Yen-Hao Chen and Yi-Yu Liu

Adaptive Cache Management for a Combined SRAM and DRAM Cache Hierarchy for Multi-cores .... 77
Fazal Hameed, Lars Bauer and Jörg Henkel

Combining RAM Technologies for Hard-error Recovery in L1 Data Caches Working at Very-low Power Modes .................................................. 83
Vicente Lorente, Alejandro Valero, Julio Sahuquillo, Salvador Petit, Ramon Canal, Pedro López and José Duato

A Dual Grain Hit-Miss Detector for Large Die-Stacked DRAM Caches .......................................................... 89
Michel El-Nacouzi, Islam Atta, Myrto Papadopoulou, Jason Zebchuk, Natalie Enright Jerger and Andreas Moshovos

Reducing Writes in Phase-Change Memory Environments by Using Efficient Cache Replacement Policies .................................................. 93
Roberto Rodríguez- Rodíguez, Fernando Castro, Daniel Chaver, Luis Pinuel and Francisco Tirado

2.5 Communications, Multimedia, and Consumer Electronics
Moderators: Theocharis Theocharides - University of Cyprus, CY; Amer Baghdadi - Telecom Bretagne/ Lab-STIC, FR

Low Complexity QR-Decomposition Architecture Using the Logarithmic Number System .................................................. 97
Jochen Rust, Frank Ludwig and Steffen Paul

Perceptual Quality Preserving SRAM Architecture for Color Motion Pictures .................................................. 103
Wen Yueh, Minki Cho and Saibal Mukhopadhyay

Parameterized Area-efficient Multi-standard Turbo Decoder .................................................. 109
Purushotham Murugappa, Amer Baghdadi and Michel Jézéquel

An H.264 Quad-Full-HD Low-Latency Intra Video Encoder .................................................. 115
Muhammad Usman Karim Khan, Jan Micha Borrmann, Lars Bauer, Muhammad Shafique and Jörg Henkel
A 100 GOPS ASP Based Baseband Processor for Wireless Communication .................................................. 121
Zhu Ziyuan, Tang Shan, Su Yongtao, Han Juan, Sun Gang and Shi Jinglin

Hardware-Software Collaborative Complexity Reduction Scheme for the Emerging HEVC Intra Encoder ................................................................. 125
Muhammad Usman Karim Khan, Muhammad Shafique, Mateus Grellert and Jörg Henkel

2.6 HOT TOPIC: Reliability Challenges of Real-time Systems in Forthcoming Technology Nodes
Organizers and Moderators: Said Hamdioui - Delft University of Technology, NL; Dimitris Gizopoulos – University of Athens, GR

Reliability Challenges of Real-Time Systems in Forthcoming Technology Nodes ........................................ 129
Said Hamdioui, Dimitris Gizopoulos, Groeseneken Guido, Michael Nicolaidis, Arnaud Grasset, Philippe Bonnot

2.7 Safety Critical Real-Time Systems
Moderators: Michael Paulitsch - EADS, DE; Giuseppe Lipari - ENS – Cachan, FR

Sensitivity Analysis for Arbitrary Activation Patterns in Real-time Systems ................................................. 135
Moritz Neukirchner, Sophie Quintan, Tobias Michaels, Philip Axer and Rolf Ernst

PT-AMC: Integrating Preemption Thresholds into Mixed-Criticality Scheduling .............................................. 141
Qingling Zhao, Zonghua Gu and Haibo Zeng

An Elastic Mixed-Criticality Task Model and Its Scheduling Algorithm .......................................................... 147
Hang Su and Dakai Zhu

An Open Platform for Mixed-Criticality Real-time Ethernet ........................................................................... 153
Gonzalo Carvajal and Sebastian Fischmeister

2.8 HOT TOPIC: IP Subsystems: The Next Productivity Wave?
Organizers and Moderators: Wido Kruijtzer - Synopsys, NL; Luciano Lavagno – Politecnico di Torino, IT

Modular SoC Integration with Subsystems: The Audio Subsystem Case ......................................................... 157
Pieter van der Wolf and Ruud Derwig

Configurability in IP Subsystems: Baseband Examples .................................................................................. 163
Pierre-Xavier Thomas, Grant Martin, David Heine, Dennis Moolenaar, and James Kim

Configurable IO Integration to Reduce System-on-Chip Time to Market: DDR, PCIe Examples ...................... 169
Frank Martin and Peter Bennett

High-performance Imaging Subsystems and Their Integration in Mobile Devices ........................................ 170
Menno Lindwer and Mark Ruvald Pedersen

3.2 PANEL: The Heritage of Mead & Conway: What Has Remained the Same, What Was Missed, What Has Changed, What Lies Ahead ......................................................... 171
Organizer: Marco Casale-Rossi - Synopsys, US
Moderators: Alberto Sangiovanni-Vincentelli - UCB, US; Marco Casale-Rossi - Synopsys, US

Panelists: Luca Carloni, Bernard Courtois, Hugo de Man, Antun Domic, and Jan Rabaey
3.3 Addressing Process and Delay Variation in High-Level Synthesis
Moderators: Lars Bauer - Karlsruhe Institute of Technology, DE; Hiroyuki Tomiyama - Ritsumeikan University, JP

Profit Maximization through Process Variation Aware High Level Synthesis with Speed Binning
Zhao Mengying, Oraloglu Alex and Xue Chun Jason

Instruction-Set Extension under Process Variation and Aging Effects
Yuko Hara-Azumi, Farshad Firouzi, Saman Kiamehr and Mehdi Tahoori

Multispeculative Additive Trees in High-Level Synthesis
Alberto A. Del Barrio, Roman Hermida, Seda Ogrenic Memik, Jose M. Mendis and Marla C. Molina

Multi-Pumping for Resource Reduction in FPGA High-Level Synthesis
Andrew Canis, Jason H. Anderson and Stephen D. Brown

Resource-Constrained High-Level Datapath Optimization in ASIP Design
Yuankai Chen and Hai Zhou

3.4 Microarchitectural Techniques for Reliability
Moderators: Todd Austin - Michigan University Ann Arbor, US; Mladen Berekovic - Technical University of Braunschweig, DE

Extracting Useful Computation from Error-Prone Processors for Streaming Applications
Yavuz Yetim, Margaret Martonosi and Sharad Malik

Orchestrator: A Low-cost Solution to Reduce Voltage Emergencies for Multi-threaded Applications
Xing Hu, Guihai Yan, Yu Hu and Xiaowei Li

Memory Array Protection: Check on Read or Check on Write?
Panagiota Nikolaou, Yiannakis Sazeides, Lorena Ndreu, Emre Özer and Sachin Idgunji

FaulTM: Error Detection and Recovery Using Hardware Transactional Memory
Gulay Yalcin, Osman Unsal and Adrian Cristal

Phoenix: Reviving MLC Blocks as SLC to Extend NAND Flash Devices Lifetime
Xavier Jimenez, David Novo and Paolo Ienne

3.5 Energy Efficient Mobile and Cloud Computing Systems
Moderators: Tajana Rosing - University of California San Diego, US; Theocharis Theocharides – University of Cyprus, CY

SCC Thermal Model Identification via Advanced Bias-Compensated Least-Squares
Roberto Diversi, Andrea Bartolini, Andrea Tilli, Francesco Beneventi and Luca Benini

System and Circuit Level Power Modeling of Energy-Efficient 3D-Stacked Wide I/O DRAMs
Karthik Chandrasekara, Christian Weis, Benny Akesson, Norbert Wehn and Kees Goossens

Design of Low Energy, High Performance Synchronous and Asynchronous 64-Point FFT

A Multi-Level Monte Carlo FPGA Accelerator for Option Pricing in the Heston Model
Christian de Schryver, Pedro Torruella and Norbert Wehn
Non-Speculative Double-Sampling Technique to Increase Energy-Efficiency in a High-Performance Processor 254
Junyoung Park, Ameya Chaudhari and Jacob A. Abraham

User-Aware Energy Efficient Streaming Strategy for Smartphone Based Video Playback Applications 258
Hao Shen and Qinru Qiu

Utility-Aware Deferred Load Balancing in the Cloud Driven by Dynamic Pricing of Electricity 262
Muhammad Abdullah Adnan and Rajesh Gupta

Leakage and Temperature Aware Server Control for Improving Energy Efficiency in Data Centers 266
Marina Zapater, José L. Ayala, José M. Moya, Kalyan Vaidyanathan, Kenny Gross and Ayse K. Coskun

3.6 Dealing with Timing Variation in Advanced Technologies
Moderators: Hans Manhaeve - Ridgetop Europe, BE; Saqib Khursheed - University of Southampton, UK

MTTF-Balanced Pipeline Design 270
Fabian Oboril and Mehdi B. Tahoori

Efficient Variation-Aware Statistical Dynamic Timing Analysis for Delay Test Applications 276
Marcus Wagner and Hans-Joachim Wunderlich

SlackProbe: A Low Overhead In Situ On-line Timing Slack Monitoring Methodology 282
Liangzhen Lai, Vikas Chandra, Robert Aitken and Puneet Gupta

Capturing Post-Silicon Variation by Layout-aware Path-delay Testing 288
Xiaolin Zhang, Jing Ye, Yu Hu and Xiaowei Li

Adaptive Reduction of the Frequency Search Space for Multi-Vdd Digital Circuits 292
Chandra K.H. Suresh, Ehder Yilmaz, Sule Ozev and Ozgur Sinanoglu

3.7 Timing Analysis
Moderators: Stefan Petters - CISTER/INESC-TEC, ISEP, PT; Michael Paulitsch - EADS, DE

FIFO Cache Analysis for WCET Estimation: A Quantitative Approach 296
Nan Guan, Xinping Yang, Mingsong Lv and Wang Yi

Timing Analysis of Multi-Mode Applications on AUTOSAR Conform Multi-Core Systems 302
Mircea Negrean, Sebastian Klawitter, Rolf Ernst

Bounding SDRAM Interference: Detailed Analysis vs. Latency-Rate Analysis 308
Hardik Shah, Alois Knoll and Benny Akesson

3.8 HOT TOPIC: Design for Variability, Manufacturability, Reliability, and Debug: Many Faces of the Same Coin?
Organizer: Vikas Chandra - ARM, US
Moderators: Vikas Chandra - ARM, US; Kartik Mohanram - University of Pittsburgh, US

Role of Design in Multiple Patterning: Technology Development, Design Enablement and Process Control 314
Rani S. Ghaida and Puneet Gupta
4.2 The Quest for Better NoCs
Moderators: Pascal Vivet - CEA-LETI, FR; Riccardo Locatelli - ST Microelectronics, FR

A Transition-Signaling Bundled Data NoC Switch Architecture for Cost-effective GALS Multicore Systems
Alberto Ghiribaldi, Davide Bertozzi and Steven M. Nowick

SMART: A Single-Cycle Reconfigurable NoC for SoC Applications
Chia-Hsin Owen Chen, Sunghyun Park, Tushar Krishna, Suvinay Subramanian, Anantha P. Chandrakasan and Li-Shiuan Peh

Switch Folding: Network-on-Chip Routers with Time-Multiplexed Output Ports
G. Dimitrakopoulos, N. Georgiadis, C. Nicopoulos and E. Kalligeros

An Efficient Network-on-Chip Architecture Based on Isolating Local and Non-Local Communications
Vahideh Akhlaghi, Mehdi Kamal, Ali Afzali-Kusha and Massoud Pedram

SVR-NoC: A Performance Analysis Tool for Network-on-Chips Using Learning-based Support Vector Regression Model
Zhiliang Qian, Da-Cheng Juan, Paul Bogdan, Chi-Ying Tsui, Diana Marculescu and Radu Marculescu

4.3 EMBEDDED TUTORIAL: Reliability Analysis Reloaded: How Will We Survive?
Organizers: Goerschwin Fey - University of Bremen, DE; Matteo Sonza Reorda - Politecnico di Torino, IT
Moderators: Bernd Becker - University of Freiburg, DE; Xavier Vera - Intel, ES

Reliability Analysis Reloaded: How Will We Survive?
Robert Aitken, Goerschwin Fey, Zbigniew T. Kalbarczyk, Frank Reichenbach, Matteo Sonza Reorda

4.4 Emerging Solutions to Manage Energy/Performance Trade-Offs along the Memory Hierarchy
Moderators: Mladen Berekovic - Technical University of Braunschweig, DE; Cristina Silvano - Politecnico di Milano, IT

MALEC: A Multiple Access Low Energy Cache
Matthias Boettcher, Giacomo Gabrielli, Bashir M. Al-Hashimi and Danny Kershaw

TreeFTL: Efficient RAM Management for High Performance of NAND Flash-based Storage Systems
Chundong Wang and Weng-Fai Wong

DA-RAID-5: A Disturb Aware Data Protection Technique for NAND Flash Storage Systems
Jie Guo, Wujie Wen, Yaojun Zhang Li, Sicheng Li, Hai Li and Yiran Chen

Exploiting Subarrays inside a Bank to Improve Phase Change Memory Performance
Jianhui Yue and Yifeng Zhu
Future of GPGPU Micro-Architectural Parameters
Cedric Nugteren, Gert-Jan van den Braak and Henk Corporaal

Synchronizing Code Execution on Ultra-Low-Power Embedded Multi-Channel Signal Analysis Platforms
Ahmed Yasir Dogan, Rubén Braojos, Jeremy Constantin, Giovanni Ansaloni, Andreas Burg and David Atienza

Using Synchronization Stalls in Power-aware Accelerators
Ali Jooya and Amirali Baniasadi

4.5 Device Identification and Protection
Moderators: Patrick Koeberl - Intel Labs, DE; Roel Maes - Intrinsic-ID, NL

Comprehensive Analysis of Software Countermeasures against Fault Attacks
Nikolaus Theifling, Dominik Merli, Michael Smola, Frederic Stumpf and Georg Sigl

An EDA-Friendly Protection Scheme against Side-Channel Attacks
Ali Galip Bayrak, Nikola Velickovic, Francesco Regazzoni, David Novo, Philip Brisk and Paolo Ienne

Design and Implementation of a Group-based RO PUF
Chi-En Yin, Gang Qu and Qiang Zhou

ClockPUF: Physical Unclonable Functions Based on Clock Networks
Yida Yao, MyungBo Kim, Jianmin Li, Igor L. Markov and Farinaz Koushanfar

Memristor PUFs: A New Generation of Memory-based Physically Unclonable Functions
Patrick Koeberl, Ünal Kocabas and Ahmad-Reza Sadeghi

Wireless Sensor Network Simulation for Security and Performance Analysis
A. Diaz, P. Sanchez, J. Sancho and J. Rico

4.6 New Techniques for Test Pattern Generation
Moderators: Sudhakar Reddy - University of Iowa, US; Matteo Sonza Reorda - Politecnico di Torino, IT

Accurate QBF-based Test Pattern Generation in Presence of Unknown Values
Stefan Hillebrecht, Michael A. Kochte, Dominik Erb, Hans-Joachim Wunderlich and Bernd Becker

Test Solution for Data Retention Faults in Low-Power SRAMs
L. B. Zordan, A. Bosio, L. Dillillo, P. Girard, A. Todri, A. Virazel and N. Badereddine

Efficient SAT-based Dynamic Compaction and Relaxation for Longest Sensitizable Paths
Matthias Sauer, Sven Reimer, Tobias Schubert, Ilia Polian and Bernd Becker

Process-Variation-Aware Iddq Diagnosis for Nano-Scale CMOS Designs - The First Step
Chia-Ling (Lynn) Chang, Charles H.-P. Wen and Jayanta Bhadra
4.7 HOT TOPIC: Security Challenges in Automotive Hardware/Software Architecture Design
Organizer: Samarjit Chakraborty - TU Munich, DE
Moderators: Jason Xue - City Univ. of Hong Kong, HK; Dip Goswami - TU Munich, DE

Security Challenges in Automotive Hardware/Software Architecture Design
Florian Sagstetter, Martin Lukasiewycz, Sebastian Steinhorst, Marko Wolf, Alexandre Bouard, William R. Harris, Somesh Jha, Thomas Peyrin, Axel Poschmann, Samarjit Chakraborty

5.1 HOT TOPIC - System Approaches to Energy-Efficiency
Organizer: Ahmed Jerraya - CEA-LETI-MINATEC, FR
Moderators: Patrick Blouet - ST Ericsson, FR; Ahmed Jerraya - CEA-LETI-MINATEC, FR

Experiences with Mobile Processors for Energy Efficient HPC
Nikola Rajovic, Alejandro Rico, James Vipond, Isaac Gelado, Nikola Puzovic and Alex Ramirez

What Designs for Coming Supercomputers?
Xavier Vigouroux

Energy-Efficient In-Memory Database Computing
Wolfgang Lehner

Performance Analysis of HPC Applications on Low-Power Embedded Platforms
Luka Stanisic, Brice Videau, Johan Cronsoie, Augustin Degomme, Vania Marangozova-Martin, Arnaud Legrand, Jean-François Méhaut

5.2 PANEL: Can Energy Harvesting Deliver Enough Power for Automotive Electronics?
Organizers: Tom Kazmierski - University of Southampton, UK; Christoph Grimm - TU Kaiserslautern, DE
Moderators: Peter Neumann - Edacentrum, DE; Norbert Wehn - TU Kaiserslautern, DE

Robert Kappel, Günter Hofer, Gerald Holweg, Thomas Herndl

Adaptable, High Performance Energy Harvesters
Paul D. Mitcheson

Ultra-Low Power: An EDA Challenge
Christoph Grimm, Javier Moreno, Xiao Pan

Tom J Kazmierski, Leran Wang, Bashir Al-Hashimi, Geoff Merrett

5.3 Post-Silicon Debug Techniques
Moderators: Jaan Raik - Tallinn University of Technology, EE; Adrian Evans - iRoC Technologies, FR

A Hybrid Approach for Fast and Accurate Trace Signal Selection for Post-Silicon Debug
Min Li and Azadeh Davoodi

Machine Learning-based Anomaly Detection for Post-silicon Bug Diagnosis
Andrew DeOrio, Qingkun Li, Matthew Burgess and Valeria Bertacco

Space Sensitive Cache Dumping for Post-silicon Validation
Sandeep Chandran, Smruti R. Sarangi and Preeti Ranjan Panda
5.4 Novel Approaches for Real-Time Architectures

A Cache Design for Probabilistically Analysable Real-time Systems ........................................... 513
Leonidas Kosmidis, Jaume Abella, Eduardo Quiñones and Francisco J. Cazorla

MARTHA: Architecture for Control and Emulation of Power Electronics and Smart Grid Systems ...... 519
Michel A. Kinsy, Ivan Celanovic, Omer Khan and Srinivas Devadas

Conservative Open-Page Policy for Mixed Time-Criticality Memory Controllers .......................... 525
Sven Goossens, Benny Akesson and Kees Goossens

An Efficient and Flexible Hardware Support for Accelerating Synchronization Operations on the STHORM Many-Core Architecture ................................................................. 531
Farhat Thabet, Yves Lhuillier, Caalph Andriamisaina, Jean-Marc Philippe and Raphaël David

5.5 Error-Aware Adaptive Modern Computing Architectures

Hot-Swapping Architecture with Back-biased Testing for Mitigation of Permanent Faults in Functional Unit Array ........................................................................................................... 535
Zoltán Endre Rákosz, Masayuki Hiromoto, Hiroshi Tsutsui, Takashi Sato, Yukihiro Nakamura and Hiroyuki Ochi

Variation-tolerant OpenMP Tasking on Tightly-coupled Processor Clusters ........................................ 541
Abbas Rahimi, Andrea Marongiu, Paolo Burgio, Rajesh K. Gupta and Luca Benini

Accurate and Efficient Reliability Estimation Techniques during ADL-Driven Embedded Processor Design ............................................................................................................................... 547
Zheng Wang, Kapil Singh, Chao Chen and Anupam Chattopadhyay

5.6 Advances in Mixed-Signal, RF, and MEMS Testing

Handling Discontinuous Effects in Modeling Spatial Correlation of Wafer-level Analog/RF Tests .......................................................... 553
Ke Huang, Nathan Kupp, John M. Carulli, Jr. and Yiorgos Makris

Fault Detection, Real-Time Error Recovery, and Experimental Demonstration for Digital Microfluidic Biochips ........................................................................................................ 559
Kai Hu, Bang-Ning Hsu, Andrew Madison, Krishnendu Chakrabarty and Richard Fair

Fault Analysis and Simulation of Large Scale Industrial Mixed-Signal Circuits ............................... 565
Ender Yilmaz, Geoff Shofner, LeRoy Winemberg and Süleyman Ozev
Electrical Calibration of Spring-Mass MEMS Capacitive Accelerometers

5.7 Compilers and Software Synthesis for Embedded Systems
Moderators: Björn Franke - University of Edinburgh, UK; Heiko Falk - Ulm University, DE

Optimizing Remote Accesses for Offloaded Kernels: Application to High-Level Synthesis for FPGA
Christophe Alias, Alain Darte and Alexandru Plesco

Sequentially Constructive Concurrency - A Conservative Extension of the Synchronous Model of Computation
Reinhard von Hanxleden, Michael Mendler, Joaquin Aguado, Björn Duderstadt, Insa Fuhrmann, Christian Motika, Stephen Mercer and Owen O'Brien

Fast and Accurate Cache Modeling in Source-Level Simulation of Embedded Software
Zhonglei Wang and Jörg Henkel

Automatic and Efficient Heap Data Management for Limited Local Memory Multicore Architectures
Ke Bai and Aviral Shrivastava

Software Enabled Wear-Leveling for Hybrid PCM Main Memory on Embedded Systems
Jingtong Hu, Qingfeng Zhuge, Chun Jason Xue, Wei-Che Tseng, and Edwin H.-M. Sha

Probabilistic Timing Analysis on Conventional Cache Designs
Leonidas Kosmidis, Charlie Curtsinger, Eduardo Quiñones, Jaume Abella, Emery Berger and Francisco J. Cazorla

6.1 EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency
Organizer: Ahmed Jerraya - CEA-LETI-MINATEC, FR
Moderators: Agnès Fritsch - Thales Group, FR; Ahmed Jerraya - CEA-LETI-MINATEC, FR

HW-SW Integration for Energy-Efficient/Variability-Aware Computing
Gasser Ayad, Andrea Acquaviva, Enrico Macili, Brahim Sahbi, Romain Lemaire

6.2 HOT TOPIC: Emerging Nanoscale Devices: A Booster for High Performance Computing
Organizers: Pierre-Emmanuel Gaillardon - EPFL, CH; Giovanni De Micheli - EPFL, CH
Moderators: Giovanni De Micheli - EPFL, CH; Ahmed Jerraya - CEA, LETI, Minatec, FR

Near-Threshold Voltage Design in Nanoscale CMOS
Vivek De

Ultra-Wide Voltage Range Designs in Fully-Depleted Silicon-On-Insulator FETs