2011 18th IEEE International Conference on Electronics, Circuits, and Systems

(ICECS 2011)

Beirut, Lebanon
11 – 14 December 2011
A1L-A1 An Efficient VLSI Implementation of H.264/AVC Intraframe Transcoder.................. 1
Michael Guarisco, Eric Dabellani, Nicolas Marques, Hassan Rabah, Yves Berviller, Serge Weber
Nancy University, France

A1L-A2 A System Approach for Reducing Power Consumption of Multimedia Devices with a Low QoE Impact................................................................. 5
Willy Aubry¹, Bertrand Le Gal¹, Dominique Dallet¹, Simon Desfarges², Daniel Négru²
¹IMS Laboratory / University of Bordeaux, France; ²LaBRI / University of Bordeaux, France

A1L-A3 Study of Interpolation Filters for Motion Estimation with Application in H.264/AVC Encoders.................................................................................... 9
Georgios Georgis, George Lentaris, Dionysios Reisis
National and Kapodistrian University of Athens, Greece

A1L-A4 HW/SW TQ/IQT Design for H.264/AVC.................................................................. 13
Ahmed Ben Atallah¹, Hassen Loukil¹, Nouri Masmoudi²
¹University of Sfax, Tunisia; ²University of Sfax / ENIS, Tunisia
A1L-B Analog Signal
Time: Monday, December 12, 10:30 - 12:00
Place: Oriana
Chair: Herve Barthelemy, Université Toulon Var

A1L-B1 Estimating the Design Value(S) of the Shunt-Peaking Inductor(S) in CMOS Trans-Impedance Amplifier System by Placement of Poles and Zeros
Rabin Raut, Aminul Talukder
Concordia University, Canada

A1L-B2 A 1.3mW CMOS 65nm 4th Order 52dB-DR Continuous-Time Analog Filter for DVB-T Receivers
Marcello De Matteis², Giuseppe Cocciolo², Marco De Biasi², Andrea Baschirotto¹
¹Università degli Studi di Milano-Bicocca, Italy; ²Università del Salento, Italy

A1L-B3 A Large Range and Fine Tuning Configurable Bandgap Reference Dedicated to Wafer-Scale Systems
Nicolas Laflamme-Mayer¹, Yves Blaquiere², Mohamad Sawan¹
¹École Polytechnique de Montréal, Canada; ²Université du Québec à Montréal, Canada

A1L-B4 Design of a Programmable Analog CMOS Rational-Powered Membership Function Generator in Current Mode Approach
Sajjad Moshfe, Abdollah Khoei, Khayrollah Hadidi, Pourya Hoseini
Urmia University, Iran

A1L-B5 Mixed Symbolic-Numerical Techniques in Fault Diagnosis Using Fault Rubber Stamps
Fawzi Al-Naima², Bessam Al-Jewad¹
¹Advanced Technology Systems Ltd., Iraq; ²Nahrain University, Iraq
A1L-C Digital Circuits
Time: Monday, December 12, 10:30 - 12:00
Place: Queen of the Colonies I
Chair: Abdallah Kassem, Notre Dame University, Lebanon

A1L-C1 An All-Digital Clock and Data Recovery Circuit for Low-to-Moderate Data Rate Applications
Ndlogou Tall², Nicolas Dehaese², Sylvain Bourdel², Bernard Bonat¹
¹DM RADIOCOM, France; ²IM2NP, France

A1L-C2 PSCML: Pseudo-Static Current Mode Logic
Yier Jin², Yiorgos Makris¹
¹University of Texas at Dallas, United States; ²Yale University, United States

A1L-C3 Adapting a C-Element Design Flow for Low Power
Matheus Moreira, Bruno Oliveira, Julian Pontes, Fernando Moraes, Ney Calazans
Pontificia Universidade do Rio Grande do Sul, Brazil

A1L-C4 Implementation of a Cost Efficient SSL Based on an Angular Beamformer SRP-PHAT
Hamid Zarghi, Mohammad Sharifkhani, Iman Gholampour
Sharif University of Technology, Iran

A1L-C5 Gate-Level Autonomous Watchdog Circuit for Error Robustness Based on a 65nm Self Synchronous System
Benjamin Devlin, Makoto Ikeda, Kunihiro Asada
University of Tokyo, Japan
A1L-D Communication Systems
Time: Monday, December 12, 10:30 - 12:00
Place: Liberty
Chair: Ahmed Eltawil, University of California, Irvine

A1L-D1 A Low-Power 2 GHz Discrete Time Weighting System Dedicated to Sampled Analog Signal Processing
Yoann Abiven¹, François Rivet¹, Yann Deval¹, Dominique Dallet¹, Didier Belot², Thierry Taris¹
¹IMS Laboratory / University of Bordeaux, France; ²STMicroelectronics, France

A1L-D2 On Provisioning High Quality in Intelligent Transportation Services
Hamada Alshaer¹, Raed Shubair¹, Thierry Ernst², Arnaud de La Fortelle²
¹Khalifa University, U.A.E.; ²Mines ParisTech, France

A1L-D3 Model-Based Design and Distributed Implementation of Bus Arbiter for Multiprocessors
Imene Ben-Hafaiedh, Susanne Graf, Mohamad Jaber
VERIMAG Laboratory, France

A1L-D4 Feed-Forward Delta Sigma Modulators Topologies Design for Broadband Communications Applications
Houda Daoud¹, Samir Ben Salem¹, Sonia Zouari², Mourad Loulou¹
¹National Engineering School of Sfax, Tunisia; ²National Engineering School of Sfax / University of Sfax, Tunisia

A1L-D5 Adaptive Digital Tanlock Loop with No Delay
Mahmoud Al-Qutayri³, Saleh Al-Araji¹, Omar Al-Ali², Nader Anani²
¹Khalifa University, U.A.E.; ²Manchester Metropolitan University, United Kingdom
A1L-E1 A 1V 115μW 20Nv/sqrtHz 15-50dB-Range PGA with 5MHz Bandwidth for UWB Personal Area Network
Marcello De Matteis¹, Marco De Blasi², Giuseppe Cocciolo³, Andrea Baschirotto², Marco Sabatini¹
¹Pirelli Tyre Spa, Italy; ²Università degli Studi di Milano-Bicocca, Italy; ³Università del Salento, Italy

A1L-E2 Sensor Node Processor for Security Applications
Goran Panic, Thomas Basmer, Oliver Schrape, Steffen Peter, Frank Vater, Klaus Tittelbach-Helmrich
IHP, Germany

A1L-E3 New Reader Anti-Collision Algorithm for Dense RFID Environments
Christine Meguerditchian, Haidar Safa, Wassim El-Hajj
American University of Beirut, Lebanon

A1L-E4 Hardware-Accelerated Address-Event Processing for High-Speed Visual Object Recognition
Michael Hofstatter, Martin Litzenberger, Daniel Matolin, Christoph Posch
Austrian Institute of Technology, Austria

A1L-E5 A Multisensor Data Fusion Approach for Improving the Classification Accuracy of Uterine EMG Signals
Bassam Moslem⁴, Mohamad Khalil², Mohamad Diab¹, Aly Chkeir³, Catherine Marque³
¹Hariri Canadian University, France; ²Lebanese University, Lebanon; ³Université de Technologie de Compiègne, France; ⁴Université de Technologie de Compiègne/Lebanese University, France
A3L-A1  1.05V 10.2mW WCDMA Analog Baseband in 65nm Digital CMOS Technology .... 97
Sergio Pernici, Pierangelo Confalonieri, Riccardo Martignone, Andrea Barbieri,
Francesca Girardi, Alessandro Mecchia, Daniele Devecchi, Germano Nicollini
ST-Ericsson, Italy

A3L-A2  High Pass Filter Implementation Comparison in Unity STF High Pass Delta
Sigma Modulator ........................................................................................................ 101
Van Tam Nguyen, Hasham Khushk, Chadi Jabbour, Patrick Loumeau
 Télécom ParisTech, France

A3L-A3  Analysis and Design of an Analog Control Loop for Digital Input Class D
Amplifiers .................................................................................................................. 105
Remy Cellier¹, Gaël Pillonnet¹, Nacer Abouchi¹, Roberto M'Rad¹, Angelo Nagar²
¹Institut des Nanotechnologies de Lyon - CPE Lyon, France; ²ST-Ericsson, France

A3L-A4  Robust Power Oscillator Design for Inductive-Power Link Applications .......... 109
Qingyun Ma, Mohammad Haider, Yehia Massoud
University of Alabama at Birmingham, United States

A3L-A5  A 2-GS/s 0.35µm SiGe Track-and-Hold Amplifier with 7-GHz Analog
Bandwidth Using a Novel Input Buffer .................................................................... 113
Damiano Cascella, Gianfranco Avitabile, Francesco Cannone, Giuseppe Coviello
Politecnico di Bari, Italy
A3L-B1 A 240mV 1MHz, 340mV 10MHz, 40nm CMOS, 252 Bits Frame Decoder Using Ultra-Low Voltage Circuit Design Platform
Sylvain Clerc, Fady Abouzeid, Fabrice Argoud, Abhay Kumar, Rajesh Kumar, Philippe Roche
STMicroelectronics, France

A3L-B2 An FPGA System Using Fuzzy Clustering and Correlation to Diagnose Angina
Evaldo Cintra, Tales Pimenta, Helton Carvalho, Robson Moreno
Universidade Federal de Itajuba, Brazil

A3L-B3 Multi-Electrode System for Pacemaker Applications
Islam Seoudi, Karima Amara, Fabrice Gayral, Renzo Dal Molin, Amara Amara
1ISEF, France; 2Sorin CRM, France

A3L-B4 Design of a Scalable DNA Shearing System Using Phased-Array Ultrasonic Transducer
Kapil Dev, Smriti Sharma, Vibhu Vivek, Babur Hadimioglu, Yehia Massoud
1Microsome Systems, United States; 2Rice University, United States; 3University of Alabama at Birmingham, United States

A3L-B5 Design of a High Efficient Fully Integrated CMOS Rectifier Using Bootstrapped Technique for Sub-Micron and Wirelessly Powered Applications
Maryam Karimi, Hooman Nabovati
Sadjad Institute of Higher Education, Iran
A3L-C1 Asymmetric Large Size Multiplication Using Embedded Blocks with Efficient Compression Technique in FPGAs
Shuli Gao, Dhamin Al-Khalili, Noureddine Chabini
Royal Military College of Canada, Canada

A3L-C2 Reversible Implementation of Square-Root Circuit
Sayeeda Sultana, Katarzyna Radecka
McGill University, Canada

A3L-C3 X86-Arm Binary Hardware Interpreter
Hussein Karaki1, Haitham Akkary1, Shahrokh Shahidzadeh2
1American University of Beirut, Lebanon; 2Intel Corporation, United States

A3L-C4 On the Impact of Encoding on the Complexity of Residue Arithmetic Circuits
Eftychios Theodorakis, Vassilis Paliouras
University of Patras, Greece

A3L-C5 An Efficient Multiple Precision Floating-Point Multiplier
Konstantinos Manolopoulos1, Dionysios Reisis2, Vassilios Chouliaras1
1Loughborough University, United Kingdom; 2National and Kapodistrian University of Athens, Greece
A3L-D1 Performance Enhancement of Single Electron Junction 1-Bit Full Adder
Iftekhar Basith, Tareq Supon, Ajit Muhury, Rashid Rashidzadeh, Majid Ahmadi
University of Windsor, Canada

A3L-D2 Impact Analysis of Stochastic Transistor Aging on Current-Steering DACs in 32nm CMOS
Simon Vanden Bussche, Pieter De Wit, Elie Maricau, Georges Gielen
KU Leuven - ESAT - Micas, Belgium

A3L-D3 Assessing Testing Techniques for Resistive-Open Defects in Nanometer CMOS Adders
Ahmed Fawaz, Ameen Jaber, Ali Kassem, Ali Chehab, Ayman Kayssi
American University of Beirut, Lebanon

A3L-D4 Hybrid Nanoparticle Biomarkers in Near-Field Optical Microscopy
Nayla Elkork1, Raed Shubair1, Paul Moretti2, Bernard Jacquier2
1Khalifa University, U.A.E.; 2Université Claude Bernard Lyon 1, France

A3L-D5 Comparison on the Performance of the Confined chalcogenide with Thin Metal Interlayer and Optimised Lateral Phase Change Memories
Santipab Sainon, Sanchai Harnsoongnoen, Chiranut Sa-Ngiamsak
Khon Kaen University, Thailand
A3L-E  Wireless Receivers
Time:  Monday, December 12, 14:30 - 16:00
Place:  Queen of the Colonies III
Chair:  François Rivet, IMS Lab

A3L-E1  Test Setup and Spurious Replicas Identification in Time-Quantized Pseudorandom Sampling-Based ADC in SDR Multistandard Receiver .......... 180
Manel Ben-Romdhane, Asma Maalej, Rihab Lahouli, Chiheb Rebai
Sup'Com, Tunisia

A3L-E2  Prefilter Bandwidth Effects in Sequential Symbol Synchronizers Based on Pulse Comparison Operating by Positive Transitions at Quarter Rate .......... 184
Antonio Reis², José F. Rocha², Atlito S. Gameiro¹, José P. Carvalho¹
¹Universidade de Aveiro, Portugal; ²University of Beira Interior, Portugal

A3L-E3  Mixed-Mode I/Q Mismatches Compensation in Low-IF Quadrature Receivers ... 188
Naveen Naraharisetti, Sleiman Bou-Sleiman, Mohammed Ismail
Ohio State University, United States

A3L-E4  Configurable Baseband Digital Transceiver for Gbps Wireless 60 GHz Communications ................................................................. 192
Dionysios Diamantopoulos², Panagiotis Galiatsatos¹, Athanasios Karachalios¹,
George Lentaris³, Dionysios Reisis¹, Dimitrios Soudris²
¹National and Kapodistrian University of Athens, Greece; ²National Technical University of Athens, Greece

A3L-E5  Fully Integrated Ultra-Low-Power 900 MHz RF Transceiver for Batteryless Wireless Microsystems ............................................. 196
Chelho Chung, Young-Han Kim, Tae-Hun Ki, Kyusung Bae, Jongbae Kim
LS Industrial Systems, Korea, South
A4P-F1 A Reliable Full-Swing Low-Distortion CMOS Bootstrapped Sampling Switch ... 200
Mohammad Reza Asgari, Seyyed Hossein Pishgar, Omid Hashemipour
SHAHD BEHESHTI UNIVERSITY, Iran

A4P-F2 On the Design of Balanced Carbon Nanotube Field-Effect Transistor Gates ..... 204
Kapil Dev¹, Yehia Massoud² ¹Rice University, United States; ²University of Alabama at Birmingham, United States

A4P-F3 Efficient Modeling and Analysis of Switch-Induced Error Voltage in High Resolution SAR ADCs ......................................................... 208
Samaneh Babayan Mashhadi¹, Seyyed Iman Pishbin² ¹Imamreza University of Mashhad, Iran; ²National Iranian Gas Company, Iran

A4P-F4 A Low Power 1-V 10-Bit 40-MS/s Pipeline ADC ................................................. 212
Mohsen Hashemi, Mohammad Sharifkhani, Mohammad Gholami
Sharif University of Technology, Iran

A4P-F5 Code-Independent Output Impedance: a New Approach to Increasing the Linearity of Current-Steering DACs ................................................. 216
Xueqing Li, Qi Wei, Huazhong Yang
Tsinghua University, China

A4P-F6 Novel Technique for Minimizing the Comparator Delay Dispersion in 65nm CMOS Technology ............................................................................... 220
Mohamed Abbas², Takahiro Yamaguchi¹, Yasuo Furukawa¹, Satoshi Komatsu², Kunihiro Asada² ¹Advantest America Corporation, Japan; ²University of Tokyo, Japan

A4P-F7 High Order Mismatch Noise Shaping for Bandpass DACs ......................................... 224
Vincent O'Brien, Brendan Mullane
University of Limerick, Ireland

A4P-F8 PSP Based DCG-FGT Transistor Model Including Characterization Procedure . 228
Abderrezak Marzaki², Virginie Bidal², Romain Laffont³, Wenceslas Rahajandraibe¹, Jean-Michel Portal¹, Rachid Bouchakour¹ ¹IM2NP, France; ²STmicroelectronics, France

A4P-F9 An Audio Band Low Voltage CT-Delta Sigma Modulator with VCO-Based Quantizer ................................................................. 232
Bahman Yousefzadeh, Mohammad Sharifkhani
Sharif University of Technology, Iran

A4P-F10 High-Pass or Low-Pass Delta Sigma Modulators? ................................................. 236
Chadi Jabbour, Hasham Khushk, Van Tam Nguyen, Patrick Loumeau
Télécom ParisTech, France

A4P-F11 Optimal Filtering of an Incremental Second-Order MASH11 Sigma-Delta Modulator ................................................................. 240
Sylvain Maréchal, François Krummenacher, Maher Kayal
École Polytechnique Fédérale de Lausanne, Switzerland

A4P-F12 A Novel Design Methodology for Multiplierless Filters Applied on Delta Sigma Decimators ......................................................... 244
Chadi Jabbour, Hussein Fakhoury, Van Tam Nguyen, Patrick Loumeau
Télécom ParisTech, France
A4P-F13 High Level Characterization and Optimization of a GPSK Modulator with Genetic Algorithm ................................................................. 248
Salwa Sahnoun1, Ahmed Fakhfakh1, N. Masmoudi1, H. Levi2
1LETI Laboratory / University of Sfax, Tunisia; 2University of Bordeaux I, France

A4P-F14 Power-Loss Reduction of a MOSFET Cross-Coupled Rectifier by Employing Zero-Voltage Switching .................................................. 252
Qingyun Ma, Mohammad Haider, Yehia Massoud
University of Alabama at Birmingham, United States

A4P-F15 A Tracking Algorithm Suitable for Embedded Systems Implementation .......... 256
Rana Farah, Qifeng Gan, Pierre Langlois, Guillaume Alexandre Bilodeau, Yvon Savaria
École Polytechnique de Montréal, Canada

A4P-F16 Performance Evaluation of Sigma Delta Zero Crossing DPLL ......................... 260
Qassim Nasir2, Saleh Al-Araji1
1Khalifa University, U.A.E.; 2University Of Sharjah, U.A.E.

A4P-F17 A 2000°/s Dynamic Range Bulk Mode Dodecagon Gyro for a Commercial SOI Technology ........................................................................ 264
Mohannad Elsayed1, Frederic Nabki2, Mourad El-Gamal1
1McGill University, Canada; 2Université du Québec à Montréal, Canada

A4P-F18 Design of a 2-Axis MEMS Accelerometer .................................................. 268
Jean Marie Darmanin, Ivan Grech, Edward Gatt, Owen Casha
University of Malta, Malta

A4P-F19 Analytical Modeling and Design of Ring Shaped Piezoelectric Transducers ..... 272
Kapil Dev2, Vibhu Vivek1, Babur Hadimioglu1, Yehia Massoud3
1Microsonic Systems, United States; 2Rice University, United States; 3University of Alabama at Birmingham, United States

A4P-F20 A Low Cost Sensing System for Foot Stress Recovering on a Freeman Platform .................................................................................. 276
Samir Boukhenous2, Mokhtar Attari1
1University of Science and Technology, Houari Boumediene, Algeria; 2University of Sciences and Technology Houari Boumediene, Algeria

A4P-F21 Fully-Integrated, Large-Time-Constant, Low-Pass, Gm-C Filter Based on Current Conveyors .................................................................... 281
Mohammad Hossein Maghami1, Amir Masoud Sodagar2
1Integrated Circuits and Systems Lab/K.N. Toosi University of Technology, Iran; 2K.N. Toosi University of Technology, Iran

A4P-F22 Stereoscopic Image Sensor with Low-Cost RGB Filters Tunned for the Visible Range .............................................................................. 285
Joao Carmo, Rui Rocha, Manuel Silva, Debora Ferreira, Joao Ribeiro, Higino Correia
Universidade do Minho, Portugal

A4P-F23 A Prototype Circuit for a Smart 3D Endoscopic VideoCapsule Based on SVM and Stereovision ............................................................... 289
Jad Ayoub1, Bertrand Granado1, Olivier Romain3, Yasser Mohanna2
1ETIS-ENSEA, France; 2Lebanese University, Lebanon; 3Université de Cergy-Pontoise / ETIS-ENSEA, France

A4P-F24 Modulation Characteristics for a Bidirectional AC-DC Converter Based on Dual Active Bridge ................................................................. 293
Karim Eduardo Hay Alonso, Abdel Karim Hay Harb, Luis David Prieto Martinez
Universidad Javeriana, Colombia
A4P-F25 Design of Ultra-Wide-Load, High-Efficient DC-DC Buck Converters ........................................... 297
Chin-Long Wey¹, Chan-I Chiu¹, Kun-Chun Chang¹, Chung-Hsien Hsu¹, Gang-Neng Sung²
¹National Central University, Taiwan; ²National Chip Implementation Center, Taiwan

A4P-F26 Mathifier - Speech Recognition of Math Equations ................................................................. 301
Salim Batlouni, Hala Karaki, Fadi Zaraket, Fadi Karameh
American University of Beirut, Lebanon

A4P-F27 Gauss-Newton Image Registration with CUDA ................................................................. 305
Manal Jalloul, Mohammed Baydoun, Mohamad Adnan Al-Alaoui
American University of Beirut, Lebanon

A4P-F28 A Random Demodulator with a Software-Based Integrator Resetting Scheme ................................ 310
Vikas Singal, Yehia Massoud
University of Alabama at Birmingham, United States

A4P-F29 Extremely Simple Constant-gm Technique for Low Voltage Rail-to-Rail Amplifier Input Stage ......................................................... 314
Boram Lee, Ted Higman
University of Minnesota, United States

A4P-F30 A Novel Frequency Compensation Scheme for on-Chip Low-Dropout Voltage Regulators ......................................................... 318
Mortaza Mojarad, Mohammad Yavari
Amirkabir University of Technology, Iran
<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
<th>Institution</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Derivative Superposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1L-A2</td>
<td>A 0.6-4.5 GHz Inductorless CMOS Low Noise Amplifier with Gyrator-C</td>
<td>Akira Kondou, Masayuki Ikebe, Junichi Motohisa, Yoshihito Amemiya, Eiichi Sano</td>
<td>Hokkaido University, Japan</td>
</tr>
<tr>
<td></td>
<td>Network</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1L-A3</td>
<td>Wideband LNA with Reactive Feedback at the Input Matching Network</td>
<td>Paria Jamshidi, Sasan Naseh</td>
<td>Ferdowsi University of Mashhad, Iran</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1L-A4</td>
<td>High Efficiency Class-E Power Amplifier with a New Output Network</td>
<td>Masoud Yavari, Sasan Naseh</td>
<td>Ferdowsi University of Mashhad, Iran</td>
</tr>
</tbody>
</table>
B1L-B Special Session 2: Modules and Systems for Multi-giga Bps 60 GHz Wireless Communications

Time: Tuesday, December 13, 09:30 - 10:40
Place: Oriana
Chair: Eric Kerherve, IMS Lab

B1L-B1 Next Generation Millimeter Wave Backhaul Radio: Overall System Design for GbE 60GHz PtP Wireless Radio of High CMOS Integration

Rodoula Makri5, Petros Tsenes5, Dimitrios Economou5, Yannis Papananos5, Dimitrios Dervenis5, Michael Birbas1, John Kikidis1, Vassilis Paliouras1, Grigoris Kalivas1, Alexis Birbas1, Panos Karaivazoglou6, Yorgos Stratakos4, John Korinthios4, Stelios Siskos2, Alkis Xatzopoulos4, John Komninos7, Serafeim Katsikas7, Konstantinos Voudouri8, Andreas Rigas6, George Agapiou6, Polivios Raxis3

1Analogies S.A., Greece; 2Aristotle University of Thessaloniki, Greece; 3Atlantis Research SA, Greece; 4Fasmetrics Ltd, Greece; 5National Technical University of Athens, Greece; 6OTE SA, Greece; 7Prisma Electronics SA, Greece; 8Sciensis Ltd., Greece; 9Technological Educational Institute of Athens, Greece; 1University of Patras, Greece

B1L-B2 Design of a 1.2-V 60 GHz Transceiver in a 90nm CMOS RF Technology

Paschalis Simitsakis3, Spiros Liolis4, Dimitris Psyllos2, Lampros Mountrichas1, Paul - Peter Sotiriadis3

1Aristotle University of Thessaloniki, Greece; 2National Technical University of Athens, Greece; 3Theta Microelectronics SA, Greece; 4University of Patras, Greece

B1L-B3 Digital Baseband Challenges for a 60GHz Gigabit Link

Nikos Kanistras3, Ioannis Tsatsaragkos3, Ahmed Mahdi3, Konstantina Karagianni3, Vassilis Paliouras3, F. Gioulekas1, E. Lalos1, K. Adaos1, Michael Birbas1, Panos Karaivazoglou2, M. Koziotis3, M. Perakis2

1Analogies S.A., Greece; 2Sciensis Ltd., Greece; 3University of Patras, Greece

B1L-B4 A 60-GHz Quadrature PLL in 90nm CMOS

Fotis Plessas1, Vasileios Panagiotopoulos3, Vasileios Kalenteridis2, George Souliotis1, Fani Liakou1, Sotiris Koutsomitsos3, Stelios Siskos2, Alexis Birbas3

1Analogies S.A., Greece; 2Aristotle University of Thessaloniki, Greece; 3University of Patras, Greece
B1L-C Circuit Level CAD
Time: Tuesday, December 13, 09:30 - 10:40
Place: Queen of the Colonies I
Chair: Rouwaida Kanj, IBM

B1L-C1 CAD Tools for Fast Analysis of Parasitic Coupling and Mismatch Effects in Switched-Capacitor Circuits ................................................................. 354
Sylvain Maréchal, François Krummenacher, Maher Kayal
École Polytechnique Fédérale de Lausanne, Switzerland

B1L-C2 SEGP-Finder: Tool for Identification of Soft Error Glitch-Propagating Paths at Gate Level ................................................................. 358
Ghailth Bany Hamad\textsuperscript{1}, Otmane Ait Mohamed\textsuperscript{1}, Syed Rafay Hasan\textsuperscript{3}, Yvon Savaria\textsuperscript{2}
\textsuperscript{1}Concordia University, Canada; \textsuperscript{2}École Polytechnique de Montréal, Canada;
\textsuperscript{3}Tennessee Technological University, United States

B1L-C3 An Evolutionary Method for Analog Circuits Optimization Utilizing Mosfet-C Filters ................................................................. 362
Badar Khan, Yaser Khalifa
State University of New York at New Paltz, United States

B1L-C4 A Greedy Algorithm for Wire Length Optimization ................................................................. 366
Yiming Li, Yi Li, Mingtian Zhou
University of Electronic Science and Technology of China, China
B1L-D FPGA Systems and Tools
Time: Tuesday, December 13, 09:30 - 10:40
Place: Liberty
Chair(s): Iyad Ouais, Lebanese American University, Lebanon
Mazen Saghir, Texas A&M University, Qatar

B1L-D1 FPGA-Based Programmable Digital PLL with Very High Frequency Resolution
Jeremy Bouloc, Laurent Nony, Christian Loppacher, Wenceslas Rahajandraibe,
Franck Bocquet, Lakhdar Zaid
IM2NP, France

B1L-D2 FPGA-Based Hardware Acceleration: a CPU/Accelerator Interface Exploration
Paulo Possa, David Schaillie, Carlos Valderrama
Université de Mons, Belgium

B1L-D3 CAD Tool for Parameterized FPGA Based FFT Architectures
Todd E. Schmuland\textsuperscript{1}, Mohsin Jamali\textsuperscript{1}, Matthew B. Longbrake\textsuperscript{2}, Peter E. Buxa\textsuperscript{2}
\textsuperscript{1}University of Toledo, United States; \textsuperscript{2}Wright-Patterson AFB, United States

B1L-D4 Customized Embedded Processor Design for Global Photographic Tone Mapping
Shervin Vakili, Diana Gil, Pierre Langlois, Yvon Savaria, Guy Bois
Ecole Polytechnique de Montréal, Canada
B1L-E  Power Electronics
Time:  Tuesday, December 13, 09:30 - 10:40
Place:  Queen of the Colonies III
Chair:  Ahmed Eltawil, University of California, Irvine

B1L-E1  A 500 mA Quiescent, 100 Ma Maximum Load CMOS Low-Dropout Regulator........ 386
John Hu\textsuperscript{1}, Brian Hu\textsuperscript{2}, Yanli Fan\textsuperscript{2}, Mohammed Ismail\textsuperscript{1}
\textsuperscript{1}Ohio State University, U.A.E.; \textsuperscript{2}Texas Instruments, United States

B1L-E2  Conducted EMI Prediction for Integrated Class D Audio Amplifier .................... 390
Roberto Mrad\textsuperscript{2}, Florent Morel\textsuperscript{1}, Gaël Pillonnet\textsuperscript{2}, Christian Vollaire\textsuperscript{1}, Angelo Nagari\textsuperscript{3}
\textsuperscript{1}Ecole Centrale de Lyon, France; \textsuperscript{2}Institut des Nanotechnologie de Lyon - CPE Lyon, France; \textsuperscript{3}ST-Ericsson, Italy

B1L-E3  A Solar Battery Charger with Maximum Power Point Tracking ......................... 394
Marc Pastre, François Krummenacher, Onur Kazanc, Naser Kosro Pour,
Catherine Pace, Stefan Rigert, Maher Kayal
École Polytechnique Fédérale de Lausanne, Switzerland

B1L-E4  Autonomous Ultra-Low Power DC/DC Converter for Microbial Fuel Cells.......... 398
Salah-Eddine Adami\textsuperscript{1}, Nicolas Degrenne\textsuperscript{1}, Christian Vollaire\textsuperscript{1}, Bruno Allard\textsuperscript{1},
François Buret\textsuperscript{1}, François Costa\textsuperscript{2}
\textsuperscript{1}Ecole Centrale de Lyon, France; \textsuperscript{2}SATIE Laboratory / University of Paris, France
B2L-A1 1.05V on-Request 10b General-Purpose ADC in 65nm Digital CMOS Technology .......................... 402
Marco Zamprogno, Alberto Minuti, Francesca Girardi, Daniele Devecchi, Germano Nicollini
ST-Ericsson, Italy

B2L-A2 A Parallel, CT-Sigma Delta Based ADC for OFDM UWB Receivers in 130 nm CMOS .......................... 406
Jokin Segundo, Jesús Arias, Luis Quintanilla, Lourdes Enríquez, Jesús M. Hernández, José Vicente
Universidad de Valladolid, Spain

B2L-A3 Design of an 8Gsp, 65nm CMOS Wideband Flash ADC .................................................. 410
Diego Mattos², Stéphane Gauffre³, Patrick Hellmuth¹, Philippe Caïs³, Jean-Louis Pedroza¹, Jean-Baptiste Bégueret², Alain Baudry⁴
¹CENBG / University of Bordeaux, France; ²IMS Laboratory / University of Bordeaux, France; ³LAB-OASU / University of Bordeaux, France; ⁴LAB-OASU, ESO / University of Bordeaux, France

B2L-A4 Dual Quantization Continuous Time Sigma Delta Modulators with Spectrally Shaped Feedback .................................................. 414
Hossein Pakniat, Mohammad Yavari
Amirkabir University of Technology, Iran

B2L-A5 A New Digital Background Correction Algorithm with Non-Precision Calibration Signals for Pipelined ADCs .......................... 418
Behzad Zeinali, Mohammad Yavari
Amirkabir University of Technology, Iran
B2L-B Nonlinear Circuits, Chaos and Complexity
Time: Tuesday, December 13, 11:00 - 12:30
Place: Oriana
Chair: Franco Maloberti, Univ of Pavia

B2L-B1 Performance Analysis of Random Demodulators with M-Sequences and Kasami Sequences
Vikas Singal, Sami Smaili, Yehia Massoud
University of Alabama at Birmingham, United States

B2L-B2 FPGA-Implementation of High-Speed MLP Neural Network
Mohammed Bahoura, Chan-Wang Park
Université du Québec à Rimouski, Canada

B2L-B3 A Hardware Efficient Chaotic Ring Oscillator Based True Random Number Generator
Ihsan Cicek, Gunhan Dundar
1Bogazici University, Turkey; 2TUBITAK UEKAE, Turkey

B2L-B4 Enhancing Synchronizability of Complex Networks by Community Weakening
Jin Fan
Donghua University, China

B2L-B5 CMOS-Compatible Structure for Voltage-Mode Multiple-Valued Logic Circuits
Mohammad Sadegh Eslampanah Sendi, Mohammad Sharifkhani, Amir Masoud Sodagar
1K.N.Toosi University of Technology, Iran; 2Sharif University of Technology, Iran
B2L-C  Arithmetic Circuits
Time:  Tuesday, December 13, 11:00 - 12:30
Place:  Queen of the Colonies I
Chair:  Amin Khajeh Djahromi, Qualcomm

B2L-C1  A1CSA: an Energy-Efficient Fast Adder Architecture for Cell-Based VLSI Design ................................................................. 442
Jucemar Monteiro¹, José Luis Güntzel³, Luciano Agostini²
¹Federal University of Santa Catarina, Brazil; ²Universidade Federal de Pelotas, Brazil; ³Universidade Federal de Santa Catarina, Brazil

B2L-C2  A Low Cost Circuit Level Fault Detection Technique to Full Adder Design........ 446
Seyyed Hasan Mozafari², Mahdi Fazeli¹, Shahin Hessabi¹, Ghassem Miremadi¹
¹Sharif University, Iran; ²Sharif University of Technology, Iran

B2L-C3  Design of New Full Adder Cell Using Hybrid-CMOS Logic Style.................. 451
Mohammad Javad Zavarei, Mohammad Reza Baghbanmanesh, Ehsan Kargaran, Hooman Nabovati, Abbas Golmakani
Sadjad Institute of Higher Education, Iran

B2L-C4  Fast Binary/Decimal Adder/Subtractor with a Novel Correction-Free BCD Addition............................................................ 455
Osama Al-Khaleel², Mohammad Al-Khaleel³, Zakaria Al-Qudah³, Christos Papachristou¹, Khaidoon Mhaidat², Francis Wolff¹
¹Case Western Reserve University, United States; ²Jordan University of Science and Technology, Jordan; ³Yarmouk University, Jordan

B2L-C5  High Speed Area Reduced 64-Bit Static Hybrid Carry-Lookahead/Carry-Select Adder........................................................................................................... 460
Habib Ghasemizadeh Tamar², Akbar Ghasemizadeh Tamar¹, Khayrollah Hadidi², Abdollah Khoei², Pouya Hoseini²
¹K.N.Toosi University of Technology, Iran; ²Urmia University, Iran
B2L-D  Sensors
Time:      Tuesday, December 13, 11:00 - 12:30
Place:     Liberty
Chair:     Mounir Boukadoum, University de Quebec, Montreal

B2L-D1 A Fully Integrated Hall Sensor Microsystem with Current-Mode Output............. 464
Andrea Ajbl, Marc Pastre, Maher Kayal
Ecole Polytechnique Federale de Lausanne, Switzerland

B2L-D2 Interface Electronics for Tactile Sensing Arrays ............................................. 468
Luigi Pinna, Giorgio Carlini, Lucia Seminara, Maurizio Valle
Università degli Studi di Genova, Italy

B2L-D3 An Improved Smart Readout Technique Based on Temporal Redundancies
Suppression Designed for Logarithmic CMOS Image Sensor........................................ 472
Hawraa Amhaz, Hassan Abbass, Hakim Zimouche, Gilles Sicard
TIMA Laboratory, France

B2L-D4 Smart Readout Design for Tactile Sensing Devices ........................................... 476
Leonardo Barboni, Maurizio Valle, Giorgio Carlini
Università degli Studi di Genova, Italy

B2L-D5 Current-Mode Motion Detector Sensor Using Copier Cell in CMOS
Technology .................................................................................................................. 480
Marcelo Macchi Da Silva3, Jacobus W. Swart3, Luiz Carlos Moreira1, Wilhelmus A.
M. Van Noije2
1Universidade Católica de Santos, Brazil; 2Universidade de São Paulo, Brazil; 3Universidade Estadual de Campinas-UNICAMP, Brazil
B2L-E1 A Self-Sufficient Digitally Controlled Ring Oscillator Compensated for Supply Voltage Variation
Mehdi Teresio, Sylvain Feruglio, Farouk Vallette, Patrick Garda, Olivier Romain, Julien Le Kernec
1Kuang-Chi Institute of Advanced Technology Shenzhen, China; 2Université de Cergy-Pontoise / ETIS-ENSEA, France; 3Université Pierre et Marie Curie - Paris 6, France

B2L-E2 A 2.4GHz Ultra-Low Power Current-Reuse Bleeding Mixer with Resistive Feedback
Hassen Kraimia, Thierry Taris, Jean-Baptiste Bégueret, Yann Deval
IMS Laboratory / University of Bordeaux, France

B2L-E3 Enabling Efficient Built-in-Self-Calibration for RFICs
Sleiman Bou-Sleiman, Mohammed Ismail
Ohio State University, United States

B2L-E4 Effective Throughput 1 Gbps-Class Millimeter-Wave Wireless System
Fumio Ozawa, Toru Taniguchi, Yasuhiro Toriyama, Jun Kobayashi, Kazuya Kojima
Japan Radio Co., Ltd., Japan

B2L-E5 A K-Band UWB CMOS Pulse-Mode Radar Transmitter
Kristian Kjelgård, Tor Sverre Lande
University of Oslo, Norway
B3L-A Special Session 3: Energy Efficient and Reconfigurable Transceivers (EERT)
Time: Tuesday, December 13, 14:00 - 15:10
Place: Lusitania
Chair: Dionysis Reisis, Univ of Athens

B3L-A1 Linear and Nonlinear Crosstalk in MIMO OFDM Transceivers
Tahereh Sadeghpour1, Raed A. Abd-Alhameed2, Nazar Thamer Ali1, I. T. E. Elfergani2, Y. A. S. Dama2, O. O. Anoh2
1Khalifa University, U.A.E.; 2University of Bradford, United Kingdom

B3L-A2 Envelope Correlation Formula for (N,N) MIMO Antenna Array Including Power Losses
Y. A. S. Dama2, Abubakar Sadiq Hussaini1, Raed A. Abd-Alhameed2, S.M.R. Jones2, Neil J. McEwan2, Tahereh Sadeghpour2, Jonathan Rodriguez1
1Instituto de Telecomunicações, Portugal; 2University of Bradford, United Kingdom

B3L-A3 Tunable RF Filters: Survey and Beyond
Abubakar Sadiq Hussaini1, Raed A. Abd-Alhameed2, Jonathan Rodriguez1
1Instituto de Telecomunicações, Portugal; 2University of Bradford, United Kingdom

B3L-A4 A Novel Dual Band Tunable Balanced Handset Antenna for WLAN Application
1Khalifa University, U.A.E.; 2University of Bradford, United Kingdom
B3L-B  Memory Circuits
Time:  Tuesday, December 13, 14:00 - 15:10
Place:  Oriana
Chair:  Amin Khajeh Djahromi, Qualcomm

B3L-B1  Memory Controller for Globally Uncoordinated and Locally Coordinated Checkpointing
Yoann Congal, Mickael Cartron
CEA, France

B3L-B2  256-KB Associativity-Reconfigurable Cache with 7T/14T SRAM for Aggressive DVS down to 0.57 V
Jinwook Jung¹, Yohei Nakata¹, Shunsuke Okumura¹, Hiroshi Kawaguchi¹,
Masahiko Yoshimoto²
¹Kobe University, Japan; ²Kobe University, JST, Japan

B3L-B3  A Novel Low Power 64-Kb SRAM Using Bit-Lines Charge-Recycling and Non-Uniform Cell Scheme
Xu Wang¹, Jianfei Jiang¹, Zhigang Mao¹, Bingjing Ge¹, Xinglong Zhao²
¹Shanghai Jiao Tong University, China; ²University of Bradford, United Kingdom

B3L-B4  A Multi-Bit Error Tolerant Register File for a High Reliable Embedded Processor
Siamak Esmaeili³, Morteza Hosseini³, Bijan Vosoughi Vahdat³, Bijan Rashidian¹
¹Sharif Univers of Technology, Iran; ³Sharif Univers of Technology, Iran
B3L-C  System Level CAD
Time:      Tuesday, December 13, 14:00 - 15:10
Place:    Queen of the Colonies I
Chair: Ricardo Reis, Universidade Federal do Rio Grande do Sul

B3L-C1 Test Data Compression Based on the Reuse of Parts of the Dictionary Entries 538
Panagiotis Sismanoglou, Dimitris Nikolos
University of Patras, Greece

B3L-C2 Automatic Generation of Memory Consistency Tests for Chip Multiprocessing 542
Eberle Rambo, Olav Henschel, Luiz C. V. Dos Santos
Universidade Federal de Santa Catarina, Brazil

B3L-C3 Efficient Periodic Clock Calculus in Latency-Insensitive Design 546
Mahdi Zare¹, Shaahin Hessabi², Maziar Goudarzi²
¹Islamic Azad University, Iran; ²Sharif University of Technology, Iran

B3L-C4 Design Space Pruning of MPSoCs Using Weighted Sub-Sampling 550
Ali Kokhazadeh, Omid Fatemi
University of Tehran, Iran
B3L-D DSP 1
Time: Tuesday, December 13, 14:00 - 15:10
Place: Liberty
Chair: Adnan Al-Alaoui, American University of Beirut, Lebanon

B3L-D1 Novel FIR Approximations of IIR Differentiators with Applications to Image Edge Detection
Mohamad Adnan Al-Alaoui
American University of Beirut, Lebanon

B3L-D2 Recursive Implementation of Exponential Linear Phase FIR Filters
Firas Hassan, Sami Khorbotly
Ohio Northern University, United States

B3L-D3 Compact Code Generation for Embedded Applications on Digital Signal Processors
Hassan Salamy
Texas State University, United States

B3L-D4 Combination of Constant Matrix Multiplication and Gate-Level Approaches for Area and Power Efficient Hybrid Radix-2 DIT FFT Realization
Sidinei Ghissoni, Eduardo Costa, Jose Monteiro, Ricardo Reis
1Inesc-Id, Portugal; 2Universidade Católica de Pelotas, Brazil; 3Universidade Federal do Rio Grande do Sul, Brazil
B4P-F1  A Wide-Frequency-Range Fractional-N Synthesizer for Clock Generation in 65nm CMOS
Ye Zhang, Niklas Zimmermann, Ralf Wunderlich, Stefan Heinen
IAS, RWTH-Aachen, Germany

B4P-F2  Design and Simulation of a Switched Capacitor Ladder Filter in a 90nm CMOS Technology for WiMAX Applications
Mohamad Reza Nazemi1, Hossein Shamsi2, Saeed Mehregan1
1Islamic Azad University, Iran; 2K.N.Toosi University of Technology, Iran

B4P-F3  Performance Evaluation of Linear and Circular Arrays in Wireless Sensor Network Localization
Ahmed Kulaib2, Raed Shubair2, Mahmoud Al-Qutayri2, Jason Ng1
1Etisalat BT Innovation Centre, U.A.E.; 2Khalifa University, U.A.E.

B4P-F4  Performance Evaluation of Distributed Tarokh SFBC and Alamouti Miso for SFN DVB-T2 Broadcast Networks
Mokhtar Tormos2, Camel Tanougast2, Abbas Dandache2, Mokhtar Tormos1, Pierre Bretillon1, Pierre Kasser1
1TDF, France; 2Université Paul Verlaine de Metz, France

B4P-F5  Performance Evaluation of Heuristic Techniques for Coverage Optimization in Femtocells
Lina Mohjazi2, Mahmoud Al-Qutayri2, Hassan Barada2, Kin Poon1
1Etisalat-BT Innovation Centre, U.A.E.; 2Khalifa University, U.A.E.

B4P-F6  Design of Low Voltage Low Power Dual-Band LNA with Forward Body Biasing Technique
AliReza Dehqan, Khalil Mafinezhad, Ehsan Kargaran, Hooman Nabovati
Sadad Institute of Higher Education, Iran

B4P-F7  Design of a CMOS LNA for the Upper Band of UWB Receivers
Abdol-Hamid Zaker1, Hossein Shamsi2, Saeed Gholami2, Mahdi Pourshamsaeie1
1Islamic Azad University, Iran; 2K.N.Toosi University of Technology, Iran

B4P-F8  A New Scheme of Coupling VCOs for the Purpose of Injection Locking Frequency Divider
Masoud Rezaei, Hassan Sepehrian, Sasan Naseh
Ferdowsi University of Mashhad, Iran

B4P-F9  The Effect of Ground Bond-Wire on the Performance of CMOS Class-E Power Amplifiers
Masoud Yavari, Sasan Naseh
Ferdowsi University of Mashhad, Iran

B4P-F10  All-Digital 400–900 MHz Power Amplifier Consuming 0.03 mW/MHz Using 0.18 µm CMOS
Sanad Bushnaq, Makoto Ikeda, Kunihiro Asada
University of Tokyo, Japan

B4P-F11  A Low Power 9GHz Divide-by-3 Injection Locked Frequency Divider in 0.18µm CMOS with 15% Locking Range
Somaye Asadian, Mohammad Jafar Hemmati, Sasan Naseh
Ferdowsi University of Mashhad, Iran
B4P-F12 Multi-User Time-Hopping IR-UWB Generator Based on FPGA with High-Speed Serial Module
Achraf Mallat, Pierre Gérard, Luc Vandendorpe
Université catholique de Louvain, Belgium

B4P-F13 Tunable Low-Pass Active Filter Using Active Capacitor for Multimode Standards
Raafat Lababidi3, Dominique Lo Hine Tong1, Ali Louzir1, Jean-Luc Robert1, Jean-Yves Le Naour1, Julien Lintignat2, Bernard Jarry2, Bruno Barelaud2
1Technicolor R&D, France; 2University of Limoges, France; 3University of Sud-Toulon - Var, France

B4P-F14 A Very Wideband Low Noise Amplifier for Cognitive Radios
Amirhossein Ansari, Mohammad Yavari
Amirkabir University of Technology, Iran
C1L-A  DSP 2  
Time: Wednesday, December 14, 09:30 - 10:30  
Place: Lusitania  
Chair: Dhamin Al-Khalili, Royal Military College, Canada  

C1L-A1  A Digital Circuit for Extracting Singular Points from Fingerprint Images .......... 627  
Rosario Arjona, Iluminada Baturone  
*Microelectronics Institute of Seville, Spain*  

C1L-A2  Combining Multiple Support Vector Machines for Boosting the Classification  
Accuracy of Uterine EMG Signals ................................................................. 631  
Bassam Moslem⁴, Mohamad Khalili², Mohamad Diab¹, Aly Chkeir², Catherine  
Marque³  
¹Hariri Canadian University, Lebanon; ²Lebanese University, Lebanon; ³Université  
de Technologie de Compiègne, France; ⁴Université de Technologie de  
Compiègne/Lebanese University, France  

C1L-A3  Fast and Flexible Genetic Algorithm Processor .............................................. 635  
Pourya Hoseini, Abdollah Khoei, Khayrollah Hadidi, Sajjad Moshfe  
*Urmia University, Iran*
C1L-B  Control Applications
Time: Wednesday, December 14, 09:30 - 10:30
Place: Oriana
Chair(s): Masoud Shafiee, Amirkabir University of Technology
Samer Saab, Lebanese American University, Lebanon

C1L-B1 Real Time Tracking Trajectory in Workspace for ANAT Robot Manipulator Using Hierarchical Control
Raouf Fareh¹, Maarouf Saad¹, Abdelkrim Brahmi¹, Mohamad Saad²
¹École de technologie supérieure, Canada; ²Université du Québec en Abitibi-Témiscamingue, Canada

C1L-B2 A New Adaptive Fuzzy FDI Method for Bond Graph Uncertain Parameters Systems
Walid Bouallegue³, Salma Bouslama Bouabdallah³, Moncef Tagina³
³L3I ENSI, Tunisia; ³LACS ENIT, Tunisia; ³University of Tunis El Manar, Tunisia
C1L-C  Reconfigurable Circuits and Networks
Time:  Wednesday, December 14, 09:30 - 10:30
Place:  Queen of the Colonies I
Chair:  Mazen Saghir, Texas A&M University, Qatar

C1L-C1  A Study on Switched-Capacitor Blocks for Reconfigurable ADCs ................................. 649
Prakash Harikumar, Anu Kalidas Muralidharan Pillai, J Jacob Wikner
Linköping University, Sweden

C1L-C2  Dynamic Routing Strategy for Embedded Distributed Architectures ......................... 653
Celine Azar¹, Stéphane Chevobbe¹, Yves Lhuillier¹, Jean-Philippe Diguet²
¹CEA, France; ²Université de Bretagne-Sud, France

C1L-C3  Controlling the Bandwidth of Bulk Acoustic Wave Filter Using a Decoder
Designed on 65nm Process ........................................................................................................... 657
Kamal Baraka¹, Eric Kerherve¹, Jean-Marie Pham¹, Moustapha El Hassan²
¹IMS Laboratory / University of Bordeaux, France; ²University of Balamand, Lebanon

C1L-C4  A 90-nm CMOS Resistor-Free Compact Trimmable Voltage Reference for
Ultra-Low Power Low Cost Applications ..................................................................................... 661
Anass Samir³, Edith Kussener³, Wenceslas Rahajandraibe¹, Ludovic Girardeau³,
Yannick Bert³, Hervé Barthélémy³
¹IM2NP, France; ³IM2NP - ISEN, France; ³STMicroelectronics, France
C1L-D Robotics
Time: Wednesday, December 14, 09:30 - 10:30
Place: Liberty
Chair: Michel Devy, LAAS-CNRS

C1L-D1 A C-Embedded Algorithm for Real-Time Monocular SLAM
Aurélien Gonzalez, Jean-Marie Codol, Michel Devy
LAAS-CNRS/Université de Toulouse, France

C1L-D2 A Non-Linear Control of Electric Vehicle Driven by Induction Motors
Djamal-Eddine Bekkouche, Khalid Hakiki, Mohammed Bouhamida, Tewfik Benabdellah
Ecole Normale Supérieure de l'Enseignement Technologique, Algeria

C1L-D3 Visual Navigation of Communicating Vehicles in Unknown and Changing Environment
David Marquez-Gamez, Michel Devy
LAAS-CNRS/Université de Toulouse, France
C2P-F Digital
Time: Wednesday, December 14, 10:50 - 11:50
Place: Pre-function Area
Chair: Iyad Ouaiss, Lebanese American University, Lebanon

C2P-F1 High Performance 4:1 Multiplexer with Ambipolar Double-Gate FETs ............ 677
Kotb Jabeur, Ian O’Connor, Nataliya Yakymets, Sébastien Le Beux
Ecole Centrale de Lyon, France

C2P-F2 A CNFET-Based Characterization Framework for Digital Circuits .................. 681
Jacques Laurent Athow2, Come Rozon2, Dhamin Al-Khalili2, Pierre Langlois1
1École Polytechnique de Montréal, Canada; 2Royal Military College of Canada, Canada

C2P-F3 A Small Footprint Interleaved Multithreaded Processor for Embedded Systems ........ 685
Charly Bechara1, Aurelien Berhault1, Nicolas Ventroux1, Stéphane Chevobbe1,
Yves Lhuillier1, Raphaël David1, Daniel Etienoble2
1CEA, France; 2Université Paris Sud - LRI, France

C2P-F4 Circuit Authentication Based on Ring-Oscillator PUFs .................................. 691
Susana Eiroa, Iluminada Baturone
Microelectronics Institute of Seville, Spain

C2P-F5 Middleware Switch ASIC Implementation .......................................................... 695
Vladimir Petrović1, Gunter Schoof1, Sergio Montenegro2
1IHP, Germany; 2University Wuerzburg, Germany

C2P-F6 FPGA Active Digital Cochlea Model ................................................................. 699
Christian Mugliette, Ivan Grech, Owen Casha, Edward Gatti, Joseph Micallef
University of Malta, Malta

C2P-F8 Cell Stack Length Using an Enhanced Logical Effort Model for a Library-Free Paradigm ......................................................... 703
Hisham El-Masry, Dhamin Al-Khalili
Royal Military College of Canada, Canada

C2P-F9 Strategic Placement of Reliable Routers for the Optimization of Dependable Dynamic NoC .......................................................... 707
Cédric Killian, Camel Tanougast, Fabrice Monteiro, Abbas Dandache
Université Paul Verlaine de Metz, France

C2P-F10 An Ultra-Fast Hybrid Simulation Framework for ASIP ....................... 711
Ji Qiu1, Xiang Gao1, Yifei Jiang1, Xu Xiao2
1Institute of Computing Technology, Chinese Academy of Sciences, China;
2University of Illinois at Urbana-Champaign, United States

C2P-F11 Power, Performance and Area Prediction of 3D ICs During Early Stage Design Exploration in 45nm ....................................................... 715
Filippos Toufexis3, Antonis Papanikolaou2, Dimitrios Soudris4, George Stamoulis4,
Sotiris Bantas1
1NCC, Greece; 2National Technical University of Athens, Greece; 3Stanford
University / National Technical University of Athens, Greece; 4University of Thessaly, Greece

C2P-F12 Fast Estimation of Memory Consumption for Energy-Efficient Compilers .......... 719
Emilio Wuerges, Romulo Silva de Oliveira, Luiz C. V. Dos Santos
Universidade Federal de Santa Catarina, Brazil

C2P-F13 System-Level Energy Estimation with Powesim .............................................. 723
Marco Giammarini, Massimo Conti, Simone Orcioni
Università Politecnica delle Marche, Italy
C2P-F14 Activity Management in Battery-Powered Embedded Systems: a Case Study of ZigBee® WSN ................................. 727
Houman Zarrabi1, Asim Al-Khalili1, Yvon Savaria2
1Concordia University, Canada; 2École Polytechnique de Montréal, Canada

C2P-F17 Rules Class Approach to Scheduling Algorithms ................................................. 732
Martin Dubois, Mounir Boukadoum
Université du Québec à Montréal, Canada

C2P-F18 High-Level Design and Synthesis of a Resource Scheduler ............................... 736
João Paulo Pizani Flor1, Tiago Rogério Mück2, Antônio Augusto Fröhlich3
1Federal University of Santa Catarina, Brazil; 2Universidade Federal de Santa Catarina, Brazil

C2P-F19 Power Consumption in Transistor Networks Versus in Standard Cells ............... 740
Gerson Scartezzini, Ricardo Reis
Universidade Federal do Rio Grande do Sul, Brazil

C2P-F20 A Higher Radix FFT FPGA Implementation Suitable for OFDM Systems ........... 744
Marwan A. Jaber, Daniel Massicotte, Youssef Achouri
Université du Québec a Trois-Rivières, Canada

C2P-F22 ILP Formulation for Hybrid FPGA MPSoCs Optimizing Performance, Area and Memory Usage .................................................. 748
Calliope-Louisa Sotiropoulou, Spyridon Nikolaidis
Aristotle University of Thessaloniki, Greece

C2P-F23 Design and Experimentation with Low-Power Morphable Multipliers .............. 752
Efstathios Sotiriou-Xanthopoulos, Dionyssios Diamantopoulos, George Economakos, Dimitrios Soudris
National Technical University of Athens, Greece

C2P-F24 A Dynamic Way Cache Locking Scheme to Improve the Predictability of Power-Aware Embedded Systems ..................................... 756
Abu Asaduzzaman3, Fadi Sibai1, Abdullah Abonamah2
1Saudi Aramco, Saudi Arabia; 2UAE Academy, U.A.E.; 3Wichita State University, United States

C2P-F25 Image Processing Technique for Segmenting Microstructural Porosity of Laser-Welded Thermoplastics ........................................... 760
Karl Leboeuf, Iman Makaremi, Roberto Muscedere, Majid Ahmadi
University of Windsor, Canada

C2P-F26 Partitioned EDF Scheduling in Multicore Systems with Quality of Service Constraints .......................................................... 764
Nadine Abdallah1, Audrey Queudeut3, Maryline Chetto1, Rafic Hage Chehade2
1IRCCyN / Université de Nantes, France; 2Lebanese University / IUT Saida, Lebanon; 3LINA / Université de Nantes, France

C2P-F27 Quality of Service Facilities for Firm Real-Time Energy Harvesting Systems ....... 768
Maissa Abdallah1, Maryline Chetto1, Audrey Queudeut3, Rafic Hage Chehade2
1IRCCyN / Université de Nantes, France; 2Lebanese University / IUT Saida, Lebanon; 3LINA / Université de Nantes, France

C2P-F28 Nonlinear Control of an Upper-Limb Exoskeleton Robot ................................... 772
Mohammad Rahman1, T K-Ouimet1, Maarouf Saad1, J.P Kenné1, Philippe Archambault2
1École de technologie supérieure, Canada; 2McGill University, Canada

Hussein El Ghor1, Maryline Chetto1, Rafic Hage Chehade2
1IRCCyN / Université de Nantes, France; 2Lebanese University, Lebanon
C2P-F30  A GPGPU-Based Software Implementation of the PBDI Deinterlacing Algorithm .............................................................. 780
Gilbert Kowarzyk, Normand Bélanger, Yvon Savaria
École Polytechnique de Montréal, Canada

C2P-F32  Performances of Switching Algorithm Methods in MIMO-OFDM Systems .......... 784
Yosra Mlayeh, Fatma Rouissi, Fethi Tilli, Adel Ghazel
Sup’Com, Tunisia

C2P-F33  Real-Time Architecture on FPGA for Obstacle Detection Using Inverse Perspective Mapping ............................................. 788
Diego Botero Galeano, Michel Devy, Jean-Louis Boizard, Wassim Filali
LAAS-CNRS/Université de Toulouse, France

C2P-F34  A Highly Accurate Fully Programmable Fuzzifier in Current Mode Approach.... 792
Sajjad Moshfe, Abdollah Khoei, Khayrollah Hadidi
Urmia University, Iran