2011 International Conference on Parallel Architectures and Compilation Techniques

(PACT 2011)

Galveston, Texas, USA
10 – 14 October 2011
2011 International Conference on Parallel Architectures and Compilation Techniques

PACT 2011

Table of Contents

Message from the General Chair .......................................................... xi
Message from the Program Chair .......................................................... xii
Conference Committees ........................................................................ xiii
Reviewers .............................................................................................. xvi

Session 2a: Scheduling

A Unified Scheduler for Recursive and Task Dataflow Parallelism ...................... 1
  Hans Vandierendonck, George Tzenakis, and Dimitrios S. Nikolopoulos

No More Backstabbing... A Faithful Scheduling Policy for Multithreaded Programs .......................................................... 12
  Kishore Kumar Pusukuri, Rajiv Gupta, and Laxmi N. Bhuyan

Dynamic Fine-Grain Scheduling of Pipeline Parallelism .................................. 22
  Daniel Sanchez, David Lo, Richard M. Yoo, Jeremy Sugerman, and Christos Kozyrakis

Session 2b: Coherence

SPATL: Honey, I Shrunk the Coherence Directory ........................................... 33
  Hongzhou Zhao, Arrvindh Shriraman, Sandhya Dwarkadas, and Vijayalakshmi Srinivasan

POPS: Coherence Protocol Optimization for Both Private and Shared Data ........ 45
  Hemayet Hossain, Sandhya Dwarkadas, and Michael C. Huang

An OpenCL Framework for Homogeneous Manycores with No Hardware Cache
  Coherence .............................................................................................. 56
  Jun Lee, Jungwon Kim, Junghyun Kim, Sangmin Seo, and Jaejin Lee

Session 3a: High-Level Programming Frameworks

Compiling Dynamic Data Structures in Python to Enable the Use of Multi-core
  and Many-core Libraries ....................................................................... 68
  Bin Ren and Gagan Agrawal

Efficient Parallel Graph Exploration on Multi-Core CPU and GPU ..................... 78
  Sungpack Hong, Tayo Oguntebi, and Kunle Olukotun
A Heterogeneous Parallel Framework for Domain-Specific Languages .........................................................89
Kevin J. Brown, Arvind K. Sujeeth, Hyuk Joong Lee, Tiark Rompf, Hassan Chaft, Martin Odersky, and Kunle Olukotun

Session 3b: Power Efficiency

PEPSC: A Power-Efficient Processor for Scientific Computing .................................................................101
Ganesh Dasika, Ankit Sethia, Trevor Mudge, and Scott Mahlke

Improving Throughput of Power-Constrained GPUs Using Dynamic Voltage/Frequency and Core Scaling ...........................................111
Jungseob Lee, Vijay Sathisha, Michael Schulte, Katherine Compton, and Nam Sung Kim

Performance Per Watt Benefits of Dynamic Core Morphing in Asymmetric Multicores ..................................121
Rance Rodrigues, Arunachalam Annamalai, Israel Koren, Sandip Kundu, and Omer Khan

Session 4: Best Paper Session

Phase-Based Application-Driven Hierarchical Power Management on the Single-chip Cloud Computer .........................................................131
Nikolas Ioannov, Michael Kauschke, Matthias Gries, and Marcelo Cintra

Optimizing Data Layouts for Parallel Computation on Multicores ...............................................................143
Yuanrui Zhang, Wei Ding, Jun Liu, and Mahmut Kandemir

DeNovo: Rethinking the Memory Hierarchy for Disciplined Parallelism .......................................................155

PACT 2011 Posters

A Hierarchical Approach to Maximizing MapReduce Efficiency .................................................................167
Zhiwei Xiao, Haibo Chen, and Binyu Zang

Building Retargetable and Efficient Compilers for Multimedia Instruction Sets ............................................169
Serge Guelton, Adrien Guinet, and Ronan Keryell

Compiler Directed Data Locality Optimization for Multicore Architectures ...............................................171
Wei Ding, Jithendra Srinivas, Mahmut Kandemir, and Mustafa Karakoy

Xin Xu and Man-Lap Li

Understanding the Behavior of Pthread Applications on Non-Uniform Cache Architectures .........................................................175
Gagandeep S. Sachdev, Kshitij Sudan, Mary W. Hall, and Rajeev Balasubramonian

Exploiting Mutual Awareness between Prefetchers and On-chip Networks in Multi-cores ...........................................177
Junghoon Lee, Minjeong Shih, Hanjoon Kim, John Kim, and Jaehyuk Huh

Decoupled Architectures as a Low-Complexity Alternative to Out-of-order Execution ..................................179
Neal C. Crago and Sanjay-J. Patel
Parameterized Micro-benchmarking: An Auto-tuning Approach for Complex Applications

Wenjing Ma, Sriram Krishnamoorthy, and Gagan Agrawal

Prediction Based DRAM Row-Buffer Management in the Many-Core Era

Manu Awashi, David W. Nellans, Rajeev Balasubramonian, and Al Davis

Program Interferometry

Zhe Wang and Daniel A. Jiménez

Regulating Locality vs. Parallelism Tradeoffs in Multiple Memory Controller Environments

Syed Minhaj Hassan, Dhiruv Choudhary, Mitchell Rasquinha, and Sudhakar Yalamanchili

Row-Buffer Reorganization: Simultaneously Improving Performance and Reducing Energy in DRAMs

Nagendra Gulur, R. Manikantan, R. Govindarajan, and Mahesh Mehendale

Scalable Proximity-Aware Cache Replication in Chip Multiprocessors

Chongmin Li, Haixia Wang, Yibo Xue, Dongsheng Wang, and Jian Li

Scalable and Efficient Bounds Checking for Large-Scale CMP Environments

Baik Song An, Ki Hwan Yum, and Eun Jung Kim

An Alternative Memory Access Scheduling in Manycore Accelerators

Yonggon Kim, Hyunseok Lee, and John Kim

Beforehand Migration on D-NUCA Caches

Javier Lira, Timothy M. Jones, Carlos Molina, and Antonio González

SymptomTM: Symptom-Based Error Detection and Recovery Using Hardware Transactional Memory

Gulay Yalcin, Osman S. Unsal, Adrian Crista!, Ibrahim Hur, and Mateo Valero

rPRAM: Exploring Redundancy Techniques to Improve Lifetime of PCM-based Main Memory

Jie Chen, Zachary Winter, Guru Venkataramani, and H. Howie Huang

Pi-TM: Pessimistic Invalidation for Scalable Lazy Hardware Transactional Memory

Anurag Negi, Per Stenstrom, Rubén Tlósz-Gil, Manuel E. Acacio, and José M. Garcia

MCFQ: Leveraging Memory-level Parallelism and Application’s Cache Friendliness for Efficient Management of Quasi-partitioned Last-level Caches

Dimitris Kaseridis, Muhammad Faisal Iqbal, Jeffrey Stuecheli, and Lisy Kurian John

MRAC: A Memristor-based Reconfigurable Framework for Adaptive Cache Replacement

Ping Zhou, Bo Zhao, Youtao Zhang, Jun Yang, and Yiran Chen
PACT 2011 SRC Posters

Sampling Temporal Touch Hint (STTH) Inclusive Cache Management Policy .......................................................... 209
  Yingying Tian and Daniel A. Jiménez

Exploiting Rank Idle Time for Scheduling Last-Level Cache Writeback ................................................................. 210
  Zhe Wang and Daniel A. Jiménez

TIDeFlow: A Parallel Execution Model for High Performance Computing Programs ....................................................... 211
  Daniel Orozco

Decoupled Cache Segmentation: Mutable Policy with Automated Bypass ................................................................. 212
  Samira Khan and Daniel A. Jiménez

A Software-Managed Coherent Memory Architecture for Manycores ................................................................. 213
  Jungho Park, Choonki Jang, and Jaejin Lee

Improving Last-Level Cache Performance by Exploiting the Concept of MRU-Tour ................................................ 214
  Alejandro Valero, Julio Sahuquillo, Salvador Petit, Pedro López, and José Duato

A Compiler-assisted Runtime-prefetching Scheme for Heterogenous Platforms .................................................... 215
  Baojiang Shou, Xiongshui Hou, and Li Chen

Improving Run-Time Scheduling for General-Purpose Parallel Code ................................................................. 216
  Alexandros Tzaimes, Rajeev Bania, and Uzi Vishkin

Collaborative Caching for Unknown Cache Sizes ........................................................................................................ 217
  Xiaoming Gu

Programming Strategies for GPUs and their Power Consumption .................................................................................. 218
  Sayan Ghosh and Barbara Chapman

An Architecture to Enable Lifetime Full Chip Testability in Chip Multiprocessors ............................................... 219
  Ranee Rodrigues, Israel Koren, and Sandip Kundu

Probabilistic Models Towards Optimal Speculation of DFA Applications ............................................................ 220
  Zhijia Zhao and Bo Wu

Session 6a: Transactional Memory

STM2: A Parallel STM for High Performance Simultaneous Multithreading Systems ................................................. 221
  Gokcen Kestor, Roberto Giro Sao, Tim Harris, Osman S. Unsal, Adrian Cristal, Ibrahim Hur,
  and Mateo Valero

Making STMs Cache Friendly with Compiler Transformations .................................................................................. 232
  Sandya Mannarswamy and Ramaswamy Govindarajan

Session 8a: Locality

Enhancing Data Locality for Dynamic Simulations through Asynchronous Data Transformations and Adaptive Control .................................................. 243
  Bo Wu, Eddy Z. Zhang, and Xipeng Shen
SFMalloc: A Lock-Free and Mostly Synchronization-Free Dynamic Memory Allocator for Manycores ................................................................. 253
Sangmin Seo, Junghyun Kim, and Jaejin Lee

Coherent Profiles: Enabling Efficient Reuse Distance Analysis of Multicore Scaling for Loop-based Parallel Programs ........................................... 264
Meng-Ju Wu and Donald Yeung

Session 8b: Customized Processors
StVEC: A Vector Instruction Extension for High Performance Stencil Computation ................................................................. 276
Naser Sedaghati, Renji Thomas, Louis-Noël Pouchet, Radu Teodorescu, and P. Sadayappan

OpenMDSP: Extending OpenMP to Program Multi-Core DSP ................................................................. 288
Jiangzhou He, Wenguang Chen, Guangri Chen, Weimin Zheng, Zhizhong Tang, and Handong Ye

ARIADNE: Agnostic Reconfiguration in a Disconnected Network Environment ................................................................. 298
Konstantinos Aisopos, Andrew DeOrio, Li-Shiuan Peh, and Valeria Bertacco

Session 9a: SPMD Analysis
Correctly Treating Synchronizations in Compiling Fine-Grained SPMD-Threaded Programs for CPU ................................................................. 310
Ziyu Guo, Eddy Zheng Zhang, and Xipeng Shen

Divergence Analysis and Optimizations ................................................................. 320
Bruno Coutinho, Diogo Sampaio, Fernando Magno Quintão Pereira, and Wagner Meira Jr.

Large Scale Verification of MPI Programs Using Lamport Clocks with Lazy Update ................................................................. 330
Anh Vo, Ganesh Gopalakrishnan, Robert M. Kirby, Bronis R. de Supinski, Martin Schultz, and Greg Bronevetsky

Session 9b: Memory Hierarchies
DiDi: Mitigating the Performance Impact of TLB Shootdowns Using a Shared TLB Directory ................................................................. 340
Carlos Villavieja, Vasileios Karakostas, Lluís Vilanova, Yoav Etzion, Alex Ramirez, Avi Mendelson, Nacho Navarro, Adrián Cristal, and Osman S. Unsal

Linear-time Modeling of Program Working Set in Shared Cache ................................................................. 350
Xiaoya Xiang, Bin Bao, Chen Ding, and Yaoqing Gao

Using a Reconfigurable L1 Data Cache for Efficient Version Management in Hardware Transactional Memory ................................................................. 361
Adrià Armejach, Azam Seyedi, Rubén Titos-Gil, Ibrahim Hur, Adrián Cristal, Osman S. Unsal, and Mateo Valero
Session 10a: Compiler Optimizations

An Evaluation of Vectorizing Compilers ................................................................. 372
  Saeed Maleki, Yaoqing Gao, Maria J. Garzaran, Tommy Wong, and David A. Padua

Modeling and Performance Evaluation of TSO-Preserving Binary Optimization ........................................ 383
  Cheng Wang and Youfeng Wu

Exploiting Task Order Information for Optimizing Sequentially Consistent Java Programs ........................................ 393
  Christoph M. Angerer and Thomas R. Gross

Session 10b: Potpourri

Memory Architecture for Integrating Emerging Memory Technologies .................................................... 403
  Kun Fang, Long Chen, Zhao Zhang, and Zhichun Zhu

Speculative Parallelization in Decoupled Look-ahead ................................................................................. 413
  Alok Garg, Raj Parihar, and Michael C. Huang

Optimizing Regular Expression Matching with SR-NFA on Multi-Core Systems ........................................ 424
  Yi-Hua E. Yang and Viktor K. Prasanna

Author Index ................................................................................................................................. 434