Innovations in Embedded and Real-Time Systems Engineering for Communication

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This article defines and analyses key challenges met in future embedded systems in networked multimedia and communication applications. Self-awareness, interoperability and embedded security are used to characterize different aspects of designing and implementing next generation embedded systems. The dynamic nature of applications and implementations as well as possible technological faults and variations need to be considered in system verification and modeling. A new design layer needs to be added to current NoC platforms in order to build procedures that take into account dynamic system reconfigurations, fault-tolerance aspects and flexible portability. Increased modularity and networked implementations create a need for trust management mechanisms between system components and technology for analyzing validity and correctness of received application and system configuration information.

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A novel master-multi-SIMD architecture and its kernel (template) based parallel programming flow is introduced as a parallel signal processing platform. The name of the platform is ePUMA (embedded Parallel DSP processor architecture with Unique Memory Access). The essential technology is to separate data accessing kernels from arithmetic computing kernels so that the run-time cost of data access can be minimized by running it in parallel with algorithm computing. The SIMD memory subsystem
architecture based on the proposed flow dramatically improves the total computing performance. The hardware system and programming flow introduced in this article will primarily aim at low-power high-performance embedded parallel computing with low silicon cost for communications and similar real-time signal processing.

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Smart devices have pervaded our society and encouraged lifestyles that depend on them. One of the fundamental requirements for a successful dependency is that the general public be aware of the energy limitations of these devices and to stay in control of energy consumption. In this paper, the authors propose a formal specification method that takes energy into account. They propose two development approaches that can use these specifications to develop energy-aware systems in a sustainable manner.

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In many kernels of multimedia applications, the working set is predictable, making it possible to schedule the data transfers before the computation. Many other kernels, however, process data that is known just before it is needed or have working sets that do not fit in the scratchpad memory. Furthermore, multimedia kernels often access two or higher dimensional data structures and conventional software caches have difficulties to exploit the data locality exhibited by these kernels. For such kernels, the authors present a Multidimensional Software Cache (MDSC), which stores 1-4 dimensional blocks to mimic in cache the organization of the data structure. Furthermore, it indexes the cache using the matrix indices rather than linear memory addresses. MDSC also makes use of the lower overhead of Direct Memory Access (DMA) list transfers and allows exploiting known data access patterns to reduce the number of accesses to the cache. The MDSC is evaluated using GLCM, providing an 8% performance improvement compared to the IBM software cache. For MC, several optimizations are presented that reduce the number of accesses to the MDSC.

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With the growing market for multi-processor system-on-chip (MPSoC) solutions, application-specific instruction-set processors (ASIPs) gain importance as they allow for a wide tradeoff between flexibility and efficiency in such a system. Their development is aided by architecture description languages (ADLs) supporting the automatic generation of architecture-specific tool sets as well as synthesizable register transfer level (RTL) implementations from a single architecture model. However, these generated implementations have to be manually adapted to the interfaces of dedicated memories or memory controllers, slowing down the design-space exploration regarding the memory architecture. To overcome this drawback, the authors extend RTL code generation from ADL models with the automatic generation of memory interfaces. This is accomplished by introducing a new abstract and versatile description format for memory interfaces and their timing protocols. The feasibility of this approach is demonstrated in real-life case studies, including a design space exploration for a banked memory system.

Section 2
Mobile Communication Applications

Chapter 6
System Architecture for 3GPP-LTE Modem using a Programmable Baseband Processor

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The evolution of third generation mobile communications toward high-speed packet access and long-term evolution is ongoing and will substantially increase the throughput with higher spectral efficiency. This paper presents the system architecture of an LTE modem based on a programmable baseband processor. The architecture includes a baseband processor that handles processing time and frequency synchronization, IFFT/FFT (up to 2048-p), channel estimation and subcarrier de-mapping. The throughput and latency requirements of a Category four User Equipment (CAT4 UE) is met by adding a MIMO symbol detector and a parallel Turbo decoder supporting H-ARQ, which brings both low silicon cost and enough flexibility to support other wireless standards. The complexity demonstrated by the modem shows the practicality and advantage of using programmable baseband processors for a single-chip LTE solution.

Chapter 7
Joint Uplink and Downlink Performance Profiling of LTE Protocol Processing on a Mobile Platform

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This article provides a detailed profiling of the layer 2 (L2) protocol processing for 3G successor Long Term Evolution (LTE). For this purpose, the most processing intensive part of the LTE L2 data plane is executed on top of a virtual ARM based mobile phone platform. The authors measure the execution times as well as the maximum data rates at different system setups. The profiling is done for uplink (UL) and downlink (DL) directions separately as well as in a joint UL and DL scenario. As a result, the authors identify time critical algorithms in the protocol stack and check to what extent state-of-the-art hardware platforms with a single-core processor and traditional hardware acceleration concepts are still applicable for protocol processing in LTE and beyond LTE mobile devices.

Chapter 8
Embedded Networks in Mobile Devices

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The concept of a mobile phone has recently transformed into a new concept of mobile multimedia devices capable of performing multiple complex tasks and integrating multiple functionalities. It has resulted in a significant increase of device integration costs and complicated deployment of new technologies. Device integrator companies favor modularity everywhere possible, which results in a new trend toward networked architectures for the mobile devices. However, comparing to the best-known embedded network solutions, e.g., SoC and NoC, these architectures have unique constraints and requirements, which also are significantly different from the wide area networks. The main constraints are power consumption and having a modular architecture to allow reuse of the components. Transition to the new architectures for mobile devices is a time consuming task that requires the analysis of many solutions applied in other contexts, especially for embedded protocols, QoS and resource management. This article reviews the state of the art in embedded networks research and the key assumptions, restrictions and limitations faced by designers of embedded networks architectures for mobile devices.

Chapter 9
Implementation of FFT on General-Purpose Architectures for FPGA

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This paper describes two general-purpose architectures targeted to Field Programmable Gate Array (FPGA) implementation. The first architecture is based on the coupling of a coarse-grain reconfigurable array with a general-purpose processor core. The second architecture is a homogeneous multi-processor system-on-chip (MP-SoC). Both architectures have been mapped onto two different Altera FPGA devices, a StratixII and a StratixIV. Although mapping onto the StratixIV results in higher operating frequencies, the capabilities of the device are not fully exploited. The implementation of a FFT on the two platforms shows a considerable speed-up in comparison with a single-processor reference architecture. The speed-up is higher in the reconfigurable solution but the MP-SoC provides an easier programming interface that is completely based on C language. The authors’ approach proves that implementing a programmable architecture on FPGA and then programming it using a high-level software language is a viable alternative to designing a dedicated hardware block with a hardware description language (HDL) and mapping it on FPGA.
Section 3
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Chapter 10
Performance Analysis of On-Chip Communication Structures under Device Variability
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On-chip communication is becoming an important bottleneck in the design and operation of high performance systems where it has to face additional challenges due to device variability. Communication structures such as tapered buffer drivers, interconnects, repeaters, and data storage elements are vulnerable to variability, which can limit the performance of the on-chip communication networks. In this regard, it becomes important to have a complete understanding of the impact that variability will have on the performance of these circuit elements in order to design high yield and reliable systems. In this paper, the authors have characterized the performance of the communication structures under the impact of random dopant fluctuation (RDF) for the future technology generations of 25, 18, and 13 nm. For accurate characterization of their performance, a Monte Carlo simulation method has been used along with predictive device models for the given technologies. Analytical models have been developed for the link failure probability of a repeater inserted interconnect which uses characterization data of all communication structures to give an accurate prediction of the link failure probability. The model has also been extended to calculate the link failure probability of a wider communication link.

Chapter 11
Schedulability Analysis for Real Time On-Chip Communication with Wormhole Switching
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In this paper, the authors discuss a real-time on-chip communication service with a priority-based wormhole switching policy. The authors present a novel off-line schedulability analysis approach, worst case network latency analysis. By evaluating diverse inter-relationships and service attributes among the traffic flows, this approach can predict the packet network latency for all practical situations. The simulation results provide evidence that communication latency calculated using the real time analysis approach is safe, closely matching the figures obtained from simulation.

Chapter 12
Modeling Communication in Multi-Processor Systems-on-Chip Using Modular Connectors
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Formal methods of concurrent programming can be used to develop and verify complex Multi-Processor Systems-On-Chip in order to ensure that these systems satisfy their functional and communication
requirements. The authors use the Action Systems formalism and show how asynchronous communication of Multi-Processor Systems-on-Chip can be modeled using generic connectors composed out of simple channel components. The paper proposes a new approach to modeling generic and hierarchical connectors for handling the complexity of on-chip communication and data flow. The authors’ goal is to avoid overloaded bus-based architectures and give a distributed framework. A case study presents the authors’ modeling methodology.

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We present an approach for generating implementations of abstraction layers implementing the communication infrastructure of applications modeled as process networks. Our approach is unique in that it does not rely on assumptions about the capabilities and topology of the underlying platform. Instead, a generic implementation is adapted to the particular platform based on information retrieved from analyzing the platform. At the heart of the approach is a novel method for analyzing the capabilities of custom execution platforms composed of components. The versatility and usefulness of the approach and analysis method is demonstrated through a case study.

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Application models are often disregarded during the design of multiprocessor Systems-on-Chip (MP-SoC). This is due to the difficulties of capturing the application constraints and applying them to the design space exploration of the platform. In this article we propose an application modelling formalism that supports joint validation of application and platform models. To support designers on the trade-off analysis between accuracy, observability, and validation speed, we show that this approach can handle the successive refinement of platform models at multiple abstraction levels. A case study of the joint validation of a single application successively mapped onto three different platform models demonstrates the applicability of the presented approach.
Chapter 15

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In this paper, the authors present a formal specification of a novel design paradigm, hierarchical agent monitored SoCs (HAMSOC). The paradigm motivates dynamic monitoring in a hierarchical and distributed manner, with adaptive agents embedded for local and global operations. Formal methods are of essential importance to the development of such a novel and complex platform. As the initial effort, functional specification is indispensable to the non-ambiguous system modeling before potential property verification. The formal specification defines the manner by which the system can be constructed with hierarchical components and the representation of run-time information in modeling entities and every type of the monitoring operations. The syntax follows the standard set theory with additional glossary and notations introduced to facilitate practical SoC design process. A case study of hierarchical monitoring for power management in NoC (Network-on-chip), written with the formal specification, is demonstrated.

Chapter 16
Service-Oriented Development of Fault Tolerant Communicating Systems: Refinement Approach

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Telecommunication systems must have a high degree of availability, that is, a high probability of correct and timely provision of requested services. To achieve this, correctness of software for such systems should be ensured. Application of formal methods helps increase confidence in building correct software. However, to be used in practice, formal methods should be well integrated into existing development process. In this paper, the authors propose a formal model-driven approach to development of communicating systems. The authors formalize and extend the Lyra approach—a top-down service-oriented method for development of communicating systems. Lyra is based on transformation and decomposition of models expressed in UML2. The authors formalize Lyra in the B Method by proposing a set of formal specification and refinement patterns reflecting the essential models and transformations of the Lyra phases. Moreover, this paper extends Lyra to integrate reasoning about fault tolerance in the entire development flow.

Compilation of References
About the Contributors
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