TABLE OF CONTENTS

SESSION 1: PLENARY SESSION 1

SESSION 2: PLENARY SESSION 2

SESSION 3A: TEST DATA & RESPONSE COMPRESSION

Not All Xs are Bad for Scan Compression ......................................................... 1
Anshuman Chandra, Rohit Kapur

Evaluation of Entropy Driven Compression Bounds on Industrial Designs ................ 7
Srinivasulu Alampally, Jais Abraham, Rabin A. Parekhji, Rohit Kapur, T.W. Williams

SESSION 3B: TEST GENERATION AND FAULT SIMULATION

Untestable Fault Identification in Sequential Circuits Using Model-Checking ................ 13
Jaan Raik, Hideo Fujiwara, Raimund Ubar, Anna Krivenko

A Test Generation Method for State-Observable FSMs to Increase Defect Coverage under the Test Length Constraint ................................................. 19
Ryoichi Inoue, Toshinori Hosokawa, Hideo Fujiwara

LIFTING: A Flexible Open-Source Fault Simulator ............................................. 27
Alberto Bosio, Giorgio Di Natale

SESSION 3C: RF TESTING

Digitally-Assisted Analog/RF Testing for Mixed-Signal SoCs .................................. 33
Hsiu-Ming (Sherman) Chang, Min-Sheng (Mitchell) Lin, Kwang-Ting (Tim) Cheng

Low-Cost One-Port Approach for Testing Integrated RF Substrates ........................ 39
Abhilash Goyal, Madhavan Swaminathan

Efficient Low-Cost Testing of Wireless OFDM Polar Transceiver Systems ................. 45
Deuk Lee, Vishwanath Natarajan, Raj Senguttuvan, Abhijit Chatterjee

SESSION 4A: TEST COMPRESSION AND BIST

Interconnect-Driven Layout-Aware Multiple Scan Tree Synthesis for Test Time, Data Compression and Routing Optimization ............................................. 51
Katherine Shu-Min Li, Jr-Yang Huang

Sequential Circuit BIST Synthesis Using Spectrum and Noise from ATPG Patterns ........ 57
Nitin Yogi, Vishwanit D. Agrawal

A Novel BIST Scheme Using Test Vectors Applied by Circuit-under-Test Itself ............... 63
Jishun Kuang, Xiong Ouyang, Zhiqiang You
SESSION 4B: TEST GENERATION FOR PHYSICAL FAULTS

XPDF-ATPG: An Efficient Test Pattern Generation for Crosstalk-Induced Faults
Sunghoon Chun, Yongjoon Kim, Taejin Kim, Myung-Hoon Yang, Sungso Kang

A Multi-valued Algebra for Capacitance Induced Crosstalk Delay Faults
Arani Sinha, Sandeep K. Gupta, Melvin A. Breuer

Increasing Defect Coverage by Generating Test Vectors for Stuck-Open Faults
Yoshinobu Higami, Kewal K. Saluja, Hiroshi Takahashi, Shin-ya Kobayashi, Yozo Takamatsu

SESSION 4C: ANALOG AND MIXED-SIGNAL TEST

Technique to Improve the Performance of Time-Interleaved A-D Converters with Mismatches of Non-linearity
Koji Asami, Hidetaka Suzuki, Hiroshki Miyajima, Tetsuya Taura, Haruo Kobayashi

A Reduced Code Linearity Test Method for Pipelined A/D Converters
Jin-Fu Lin, Te-Chieh Kang, Soon-Jyh Chang

Testing LCD Source Driver IC with Built-on-Scribe-Line Test Circuitry
Jui-Jer Huang, Chiuan-Che Li, Jinn-Lang Huang

SESSION 5A: DELAY TESTING

Identifying Non-Robust Untestable RTL Paths in Circuits with Multi-cycle Paths
Thomas Edison Yu, Tomokazu Yoneda, Satoshi Ohtake, Hideo Fujiwara

High Quality Pattern Generation for Delay Defects with Functional Sensitized Paths
Ming-Ting Hsieh, Shun-Yen Lu, Jing-Jia Liou, Augusti Kifli

Refining Delay Test Methodology Using Knowledge of Asymmetric Transition Delay
Sean H. Wu, Sreejit Chakravarty, Alexander Tetelbaum, Li-C. Wang

SESSION 5B: SPECIAL SESSION: ANALOG PRODUCTION TEST 1

Effects of Advances in Analog, Mixed Signal and IO Circuits on Test Strategies
Salem Abdennadher

Electrical Overstress Prevention & Test Best Practices
Leslie Khoo

Low Distortion Sine Waveform Generation by an AWG
Akinori Maeda

SESSION 5C: HYBRID METHOD FOR TEST DATA COMPRESSION

An Effective Hybrid Test Data Compression Method Using Scan Chain Compaction and Dictionary-Based Scheme
Taejin Kim, Sunghoon Chun, Yongjoon Kim, Myung-Hoon Yang, Sungso Kang

Optimizing Test Data Volume Using Hybrid Compression
Brton Keller, Sandeep Bhatia, Thomas Bartenstein, Brian Foutz, Anis Uzzaman
Cost Efficient Methods to Improve Performance of Broadcast Scan
Seongmoon Wang, Wenlong Wei

SESSION 6A: FAULT DIAGNOSIS

Hyperactive Faults Dictionary to Increase Diagnosis Throughput
Chen Liu, Wu-Tung Cheng, Huaxing Tang, Sudhakar M. Reddy, Wei Zou, Manish Sharma

Enhancing Transition Fault Model for Delay Defect Diagnosis
Wu-Tung Cheng, Brady Benware, Ruifeng Guo, Kun-Han Tsai, Takeo Kobayashi, Kazuyuki Maruo, Michinobu Nakao, Yoshitaki Fukui, Hideyuki Otake

Observation Point Oriented Deterministic Diagnosis Pattern Generation (DDPG) for Chain Diagnosis
Fei Wang, Yu Hu, Yu Huang, Jing Ye, Xiaowei Li

SESSION 6B: SPECIAL SESSION: ANALOG PRODUCTION TEST 2

The HiZ Problem of Power Management IC Testing
Hagen Goller

Total Jitter Measurement for Testing HSIO Integrated SoCs
Takahiro J. Yamaguchi, Masahiro Ishida

Load-Board/PCB Noise Suppression via Electromagnetic Band Gap Power Plane Patterning
Fidel Muradali, Suzanne Huh, Madhavan Swaminathan

SESSION 6C: DEFECT BASED TESTING

Defect Detection Rate through IDDQ for Production Testing
Junichi Hirase

Variation Aware Analysis of Bridging Fault Testing
Urban Ingelsson, Bashir M. Al-Hashimi, Peter Harrod

Prioritizing the Application of DFM Guidelines Based on the Detectability of Systematic Defects
Dongok Kim, Irith Pomeranz, M. Enamul Amyeen, Srikanth Venkataraman

SESSION 7A: PANEL: HOW TO INCREASE THE EFFECTIVENESS OF YIELD DIAGNOSTICS- IS DFM THE ANSWER TO THIS?

How To Increase the Effectiveness of Yield Diagnostics-Is DFM the Answer to This?
Anis Uzzaman

SESSION 7B: POWER AWARE TEST GENERATION

Targeting Leakage Constraints during ATPG
Görschwin Fey, Satoshi Komatsu, Tasuo Furukawa, Masahiro Fujita
Power Management for Wafer-Level Test During Burn-In
Sudarshan Bahukudumbi, Krishnendu Chakrabarty

Test Generation for State Retention Logic
Krishna Chakravadhanula, Vivek Chickermane, Briton Keller, Patrick Gallagher, Steven Gregor

SESSION 7C: DESIGN FOR EFFICIENT TEST

Area and Test Cost Reduction for On-Chip Wireless Test Channels with System-Level Design Techniques
Chun-Kai Hsu, Li-Ming Deng, Mao-Yin Wang, Jing-Jia Liou, Chih-Tsun Huang, Cheng-Wen Wu

On-Chip Test Generation Mechanism for Scan-Based Two-Pattern Tests
Nan-Cheng Lai, Sying-Jyan Wang

Level-Testability of Multi-operand Adders
Nobutaka Kito, Naofumi Takagi

SESSION 8A: INDUSTRY SESSION

System Level LBIST Implementation
Fei Zhuang, JunBo Jia, Xiangfeng Li

CoolLBIST: An Effective Approach of Test Power Reduction for LBIST
Jun Matsushima, Yoichi Maeda, Masahiro Takakura

Practical Challenges in Logic BIST Implementation – Case Studies
Shianling Wu, Hiroshi Furukawa, Boryau Sheu, Laung-Terng Wang, Hao-Jan Chao, Lishen Yu, Xiaoqing Wen, Michio Murakami

USB2.0 Logic Built In Self Test Methodology
Kean Hong Boey, Kok Sing Yap, Wai Mun Ng

Shared At-Speed BIST for Parallel Test of SRAMs with Different Address Sizes
Tomonori Sasaki, Yoshiyuki Nakamura, Toshiharu Asaka

Experimental Results of Built-In Jitter Measurement for Gigahertz Clock
Nai-Chen Daniel Cheng, Yu Lee, Ji-Jan Chen

Leading Edge Technology and Test Noise
Katayama Takayuki, Kou Ebihara, Goro Imamrzi

DFT Technique to Conclusively Translate Floating Nodes to High IDDQ Current in Analog Circuits
Ricky Smith, Jiang Shi

Diagnosis of Voltage Dependent Scan Chain Failure Using VBUMP Scan Debug Method
Khairul Khuyyari, Wei Tee Ng, Neal Jaarsma, Robert Abraham, Peng Weng Ng, Boon Huai Ang, Chin Huong

Detectability of the Two-Dimensional Detector for Time Resolved Emission Measurement
Nobuyuki Hirai

Protocol Aware Test Methodologies Using Today’s ATE
Shawn Molavi, Andy Evans, Ray Clancy
SESSION 8B: SOC TEST

Core-Level Compression Technique Selection and SOC Test Architecture Design ........................................... 233
Anders Larsson, Xin Zhang, Erik Larsson, Krishnendu Chakrabarty

Simulation-Driven Thermal-Safe Test Time Minimization for System-on-Chip ............................................. 239
Zhiyuan He, Zeho Peng, Petra Eles

A Design-for-Debug (DFD) for NoC-Based SoC Debugging via NoC ......................................................... 245
Hyunbean Yi, Sungju Park, Sandip Kundu

Accelerated Functional Testing of Digital Microfluidic Biochips .............................................................. 251
Debasis Mitra, Sarmishtha Ghoshal, Hafizur Rahaman, Bhargab B. Bhattacharya, D. Dutta,
Majumder, Krishnendu Chakrabarty

SESSION 8C: DESIGN VERIFICATION AND VALIDATION

On Reusing Test Access Mechanisms for Debug Data Transfer in SoC Post-Silicon Validation .................................................. 257
Xiao Liu, Qiang Xu

A Robust Automated Scan Pattern Mismatch Debugger ................................................................. 263
Kun-Han Tsai, Ruifeng Guo, Wu-Tung Cheng

An Interactive Verification and Debugging Environment by Concrete/Symbolic Simulations for System-Level Designs .................................. 269
Yoshihisa Kojima, Tasuku Nishihara, Takeshi Matsumoto, Masahiro Fujita

Coverage Directed Test Generation: Godson Experience ................................................................. 275
Haihua Shen, Wenli Wei, Yunji Chen, Bowen Chen, Qi Guo

SESSION 9A: POWER AWARE SCAN TEST

Test Power Reduction by Blocking Scan Cell Outputs ............................................................................... 281
Xijiang Lin, Janusz Rajski

Two-Gear Low-Power Scan Test ............................................................................................................. 289
Chao-Wen Tzeng, Shi-Yu Huang

DCScan: A Power-Aware Scan Testing Architecture ............................................................................... 295
Gui Dai, Zhiqiang You, Jiaxin Kuang, Jiedi Huang

SESSION 9B: MEMORY SELF TEST

Layout-Aware and Programmable Memory BIST Synthesis for Nanoscale System-on-Chip Designs .................................................................................. 301
Aman Kekrady, C.P. Ravikumar, Nitin Chandrachoodan

A Low-Cost Pipelined BIST Scheme for Homogeneous RAMs in Multicore Chips ............................................. 307
Yu-Jen Huang, Jin-Fu Li

A Software-Based Test Methodology for Direct-Mapped Data Cache ......................................................... 313
Yi-Cheng Lin, Yi-Ying Tsai, Kuei-Jong Lee, Cheng-Wei Yan, Chung-Ho Chan
SESSION 9C: ON-LINE TEST

Time-Multiplexed Online Checking: A Feasibility Study .................................................. 319
Ming Gao, Hsiu-Ming (Sherman) Chang, Peter Lisherness, Kwang-Ting (Tim) Cheng

On-Line Instruction-Checking in Pipelined Microprocessors ........................................... 325
Stefano Di Carlo, Giorgio Di Natale, Riccardo Mariani

Design of FSM with Concurrent Error Detection Based on Viterbi Decoding ..................... 331
Li Ming, Xu Shiyi, Xia Enjun, Wan Feyu

SESSION 10A: POWER AWARE DELAY TESTING

PHS-Fill: A Low Power Supply Noise Test Pattern Generation Technique for At-Speed
Scan Testing in Huffman Coding Test Compression Environment ................................... 337
Yi-Taung Lin, Meng-Fan Wu, Jian-Lang Huang

CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme for Reducing Yield
Loss Risk in At-Speed Scan Testing .................................................................................. 343

Power Analysis and Reduction Techniques for Transition Fault Testing ............................. 349
Khushboo Agarwal, Srinivas Vooka, Srivaths Ravi, Rubin Parekhji, Arjun Singh Gill

SESSION 10B: ADVANCED MEMORY TEST

Influence of Parasitic Capacitance Variations on 65 nm and 32 nm Predictive Technology
Model SRAM Core-Cells ........................................................................................................ 355
Stefano Di Carlo, Alessandro Savino, Alberto Scionti, Paolo Prinetto

Test and Diagnosis Algorithm Generation and Evaluation for MRAM Write Disturbance
Faults ...................................................................................................................................... 361
Wan-Yu Lo, Ching-Yi Chen, Chin-Lang Su, Cheng-Wen Wu

GDDR5 Training – Challenges and Solutions for ATE-Based Test .................................... 367
Hubert Werkmann, Dong-Myong Kim, Shinji Fujita

SESSION 10C: FAULT TOLERANCE AND DEPENDABLE SYSTEM

A Re-design Technique for Datapath Modules in Error Tolerant Applications .................... 373
Doochul Shin, Sandeep K. Gupta

Reliable Network-on-Chip Router for Crosstalk and Soft Error Tolerance .......................... 380
Ying Zhang, Huawei Li, Xiaowei Li

Analyses on Trend of Accidents in Financial Information Systems Reported by
Newspapers from the Viewpoint of Dependability ............................................................... 386
Koichi Bando, Kenji Tanaka

Author Index