Table of Contents

Preface

Chapter 1
Interface Characterization

Fluctuations in Electronic Properties of MOS Interface in Nanoscale MOSFETs
T. Tsuchiya, Y. Morimura, and Y. Mori

Electron States in MOS Systems
O. Engström

Process Engineering and Trap Distribution for Dielectric/Si Interfacial Layer in High-k Gated MOS Devices
K. Chang-Liao, C. Fu, C. Lu, Y. Chang, Y. Hsu, C. Tsao, T. Wang, D. Heh, Y. Li, W. Tsai, C. Ai, F. Hou, and Y. Hsu

Current Understanding of the Transport Behavior of Hydrogen Species in MOS Stacks and Their Relation to Reliability Degradation
Z. Liu, S. Fujieda, H. Ishigaki, M. Wilde, and K. Fukutani

Impact of Silicon Nitride Gate Dielectric Composition on the Stability of Low Temperature Nanocrystalline Silicon Thin Film Transistors
M. Esmaeili-Rad, G. Chaji, F. Li, M. Moradi, A. Sazonov, and A. Nathan

Development of a Fast Technique for Characterizing Interface States
L. Lin, Z. Ji, J. Zhang, and W. Zhang

Detailed Analysis of Si-SiO2 Interface Traps in State-of-the-Art MOSFETs Using Charge Pumping
D. Bauza

Clear Difference between the Chemical Structure of SiO2/Si Interfaces Formed Using Oxygen Radicals versus Oxygen Molecules
T. Suwa, Y. Kumagai, A. Teramoto, T. Muro, T. Kinoshita, T. Ohmi, and T. Hattori
Chapter 2
Ultra-Thin Film/Reliability

Impact of Twofold Coordinated Nitrogen on the Generation of Deep-Level Hole Traps under Negative-Bias Temperature Stressing
C. Gu, D. Ang, and Z. Teo

Essential aspects of Negative Bias Temperature Instability (NBTI)
A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta, and M. Alam

Atomic Imaging of Atomic H Cleaning of InGaAs and InP for ALD
W. Melitz, J. Shen, T. Kent, R. Droopad, P. Hurley, and A. C. Kummel

Plasma-Assisted Atomic Layer Deposition of Low Temperature SiO$_2$
G. Dingemans, C. Van Helvoirt, M. Van de Sanden, and W. M. Kessels

Surface Passivation of InGaAs/InP HBTs Using Atomic Layer Deposited Al$_2$O$_3$
R. Driad, F. Benkhelifa, L. Kirste, R. Lösch, M. Mikulla, and O. Ambacher

Nitric Acid Oxidation Method to Form a Gate Oxide Layer in Sub-Micrometer TFT
T. Matsumoto, Y. Kubota, S. Imai, and H. Kobayashi

Effects of Deposition Method of PECVD Silicon Nitride as MIM Capacitor Dielectric for GaAs HBT Technology
J. Yota

Low Temperature Processing of Si-Based Dielectric Thin Films
P. Joshi, A. Voutsas, and J. Hartzell

Negative Charge in Plasma Oxidized SiO$_2$ Layers
A. Boogaard, A. Y. Kovalgin, and R. Wolters

Optical and Electrical Properties of Si-Based Multilayer Structures for Solar Cell Applications
R. Nalini, J. Cardin, K. R. Dey, X. Portier, C. Dufour, and F. Gourbilleau

Context Dependence Effects in Si/SiON Based Advanced CMOS Devices
O. O. Olubuyide

Quantitative Discussion on Electron-Hole Universal Tunnel Mass in Ultrathin Dielectric of Oxide and Oxide-Nitride
H. Watanabe
Physics-Based Hot-Carrier Degradation Modeling
321

Intrinsic Variability and Reliability in Nano-CMOS
J. Velamala, C. Wang, R. Zheng, Y. Ye, and Y. Cao
353

Bias-Temperature Instabilities and Radiation Effects on SiC MOSFETs
369

Chapter 3
Emerging Dielectrics

Impact of Gate Dielectric Geometry on the Nanowire MOSFETs Performance and Scaling
M. Li, W. Cao, D. Huang, C. Shen, S. Cheng, C. Yao, and H. Yu
383

Role of Oxygen Transfer for High-k/SiO2/Si Stack Structure on Flatband Voltage Shift
T. Nabatame, A. Ohi, and T. Chikyow
403

Charge Trapping and Reliability Properties of MONOS Memory with High-k Blocking Layer
N. Yasuda, S. Fujii, J. Fujiki, and H. Kusai
417

Dynamic Negative Bias Stress Instability Effects in Hafnium Silicon Oxynitride and Silicon Dioxide
J. Mee, R. Devine, H. Hjalmarson, and K. Kambour
447

Electrical and Structural Properties of Ternary Rare-Earth Oxides on Si and Higher Mobility Substrates and their Integration as High-k Gate Dielectrics in MOSFET Devices
461

High-k Integration and Interface Engineering for III-V MOSFETs
H. Oh, A. B. Sumartina, and S. Lee
481

Plasma Enhanced Atomic Layer Deposition of ZrO2: A Thermodynamic Approach
E. Blanquet, D. Monnier, I. Nuta, F. Volpi, B. Doisneau, S. Coindeau, J. Ray, B. Detlefs, Y. Mi, J. Zegenhagen, C. Martinet, C. Wyon, and M. Gros-Jean
497
V1 Stability Of High-K/Metal Gate Stacks with Device Scaling in 30nm FDSOI Technology
X. Garros, L. Brunet, M. Cassé, O. Weber, F. Andrieu, D. Lafond, C. Gaumer, G. Reimbold, and F. Boulanger

Investigation of Electron and Hole Charge Trapping in LaLuO3 Stack MOS Capacitor Using the 3-Pulse CV Technique
N. Sedghi, I. Mitrovic, J. Lopes, J. Schubert, and S. Hall

Inelastic Electron Tunneling Spectroscopy (IETS) Study of Ultra-Thin Gate Dielectrics for Advanced CMOS Technology
T. Ma

High-k Gate Dielectric MOSFETs: Meeting the Challenges of Characterization and Modeling
M. M. De Souza, S. Sicre, and D. Casterman

Universal Set/Reset Characteristics of Metal-Oxide Resistance Switching Memories
D. Ielmini

Resistive Switching Behaviors of ReRAM Having W/CeO2/Si/TiN Structures

Electrically Detected Magnetic Resonance in Dielectric Semiconductor Systems of Current Interest
P. M. Lenahan, C. Cochrane, J. Campbell, and J. Ryan

Synthesis, Pore Morphology, and Dielectric Property of Mesoporous Low-k Material PSMSQ Using a Reactive High-Temperature Porogen, TEPSS
S. Chiu, H. Hsu, M. Che, and J. Leu

Electrical Characteristics Analysis at "Oxide Flat-Band Voltage" for Al-SiO2-Si Capacitor
H. Lu, T. Chen, and J. Hwu

Novel Hardmask for Sub-20nm Copper/Low K Backend Dual Damascene Integration
L. Xia, Z. Cui, M. Balseanu, V. Nguyen, K. Zhou, J. Pender, and M. Naik

Study of Porous SiOCH Patterning Using Metallic Hard Mask: Challenges and Solutions

Process Challenges for Integration of Copper Interconnects with Low-k Dielectrics
J. Gambino
Chapter 4
Poster Session

Schottky Barrier Height at Dielectric Barrier/Cu Interface in Low-K/Cu Interconnects
S. King, M. French, M. Jaehnig, M. Kuhn, and B. French

xi
Global and Local Stress Characterization of SiN/Si(100) Wafers Using Optical Surface Profilometer and Multiwavelength Raman Spectroscopy

W. Yoo, J. Kajiwara, T. Ueda, T. Ishigaki, and K. Kang

Mechanisms of Difficulty to Correlate the Leakage Current of High-k Capacitor Structures with Defect States Detected Spectroscopically by the Thermally Stimulated Current Technique

W. S. Lau

Degradation Mechanisms of MILC P-Channel Poly-Si TFTs under Dynamic Hot-Carrier Stress Using a Novel Test Structure

C. Lin, W. Hong, T. Lin, H. Lin, and T. Huang

Solution Processed High-k Lanthanide Oxides for Low Voltage Driven Transparent Oxide Semiconductor Thin Film Transistors

S. Choi, B. Park, M. Jang, S. Jeong, J. Lee, B. Ryu, T. Seong, and H. Jung

Reliability Properties and Current Conduction Mechanisms of HfO2 MIS Capacitor with Dual Plasma Treatment

K. Chang, T. Chang, S. Chen, and I. Deng

A MIM Diode with Ultra Abrupt Switching Process and High On/Off Current Ratio

L. Zhang and R. Huang

Author Index