# Table of Contents

FPGA 2010 Symposium Organization ............................................................................................................. ix

Pre-Conference Workshop

- **FPGA-2010 Pre-Conference Workshop on Open-Source for FPGA** ..................................................... 1
  Shep Siegel (Atomic Rules LLC), Mike Wirthlin (Brigham Young University)

Session 1: SoC Implementation

- **Intel® Nehalem Processor Core Made FPGA Synthesizable** ................................................................. 3
  Graham Schelle, Jamison Collins, Ethan Schuchman, Perry Wang, Xiang Zou, Gautham Chinya,
  Ralf Plate, Thorsten Mattner, Franz Olbrich, Per Hammarlund, Ronak Singhal, Jim Brayton,
  Sebastian Steibl, Hong Wang (Intel Corporation)

- **FPGA Prototyping of an AMBA-Based Windows-Compatible SoC** .................................................... 13
  Kan Huang, Junlin Lu, Jiu Feng Pang, Yansong Zheng, Hao Li, Dong Tong, Xu Cheng (Peking University)

- **Predicting the Performance of Application-Specific NoCs Implemented on FPGAs** ......................... 23
  Jason Lee, Lesley Shannon (Simon Fraser University)

- **Combining Multicore and Reconfigurable Instruction Set Extensions** ............................................... 33
  Zhimin Chen (Virginia Polytechnic Institute), Richard Neil Pittman, Alessandro Forin (Microsoft Research)

- **Energy Efficient Sensor Node Implementations** .................................................................................... 37
  Jan R. Frigo, Eric Y. Raby, Sean M. Brennan (Los Alamos National Laboratory),
  Christophe Wolinski, Charles Wagner, Francois Charot (University of Rennes),
  Edward Rosten (University of Cambridge), Vinod K. Kulathumani (West Virginia University)

Session 2: High-Level Synthesis

- **Efficient Multi-Ported Memories for FPGAs** ....................................................................................... 41
  Charles Eric LaForest, J. Gregory Steffan (University of Toronto)

- **Automatic Generation of High-Performance Multipliers for FPGAs with Asymmetric Multiplier Blocks** 51
  Shreesha Srinath, Catherine Compton (University of Wisconsin-Madison)

- **Bit-Level Optimization for High-Level Synthesis and FPGA-Based Acceleration** .............................. 59
  Jiyu Zhang (Peking University & University of California, Los Angeles),
  Zhiru Zhang, Sheng Zhou (AutoESL Design Technologies),
  Mingxing Tan, Xianhua Liu, Xu Cheng (Peking University),
  Jason Cong (University of California, Los Angeles & UCLA/PKU Joint Research Institute in Science and Engineering),

- **Designing Hardware with Dynamic Memory Abstraction** ................................................................. 69
  Jiri Simsa (Carnegie Mellon University), Satnam Singh (Microsoft Research UK)

Session 3: Acceleration Engines

- **High-Throughput Bayesian Computing Machine with Reconfigurable Hardware** ............................ 73
  Mingjie Lin, Iliia Lebedev, John Wawrzynk (University of California, Berkeley)

- **High Throughput and Large Capacity Pipelined Dynamic Search Tree on FPGA** .............................. 83
  Yi-Hua Edward Yang, Viktor K. Prasanna (University of Southern California)

- **FPMR: MapReduce Framework on FPGA: A Case Study of RankBoost Acceleration** ...................... 93
  Yi Shan, Bo Wang, Jing Yan, Yu Wang (Tsinghua University & Microsoft Research Asia),
  Ningyi Xu (Microsoft Research Asia), Huazhong Yang (Tsinghua University)

- **Acceleration of an Analytical Approach to Collateralized Debt Obligation Pricing** ......................... 103
  Dharmendra P. Gupta, Paul Chow (University of Toronto)
• A 3D-Audio Reconfigurable Processor ......................................................... 107
  Dimitris Theodoropoulos, Georgi Kuzmanov, Georgi Gaydadjiev (Delft University of Technology)

• Accelerating Monte Carlo Based SSTA Using FPGA .................................... 111
  Jason Cong, Karthik Gururaj, Wei Jiang, Bin Liu, Kirill Minkovich, Bo Yuan, Yi Zou
  (University of California, Los Angeles)

Session 4: Reconfigurable Computing Systems

• Axel: A Heterogeneous Cluster with FPGAs and GPUs .................................. 115
  Kuen Hung Tsai, Wayne Luk (Imperial College London)

• Server-Side Coprocessor Updating for Mobile Devices with FPGAs .................. 125
  Chen Huang, Frank Vahid (University of California, Riverside)

• Accurately Evaluating Application Performance in Simulated Hybrid Multi-Tasking Systems ................................................................. 135
  Kyle Rupnow, Jacob Adriaens, Wenyn Fu, Katherine Compton (University of Wisconsin-Madison)

Panel

• FPGA’10 Panel: Programming High Performance Signal Processing Systems in High Level Languages ................................................................. 145
  Kees Vissers (Xilinx), Devadas Varma (AutoESL), Vinod Kathail (Synfora), Jeff Bier (BDTI), Don MacMillen (Stretch, Inc.), Joseph Cavallaro (Rice University)

Session 5: CAD Tools

• Towards Scalable Placement for FPGAs ...................................................... 147
  Huimin Bian, Andrew C. Ling, Alexander Choong, Jianwen Zhu (University of Toronto)

• FPGA Power Reduction by Guarded Evaluation ............................................. 157
  Jason H. Anderson, Ching Ravishankar (University of Toronto)

• A Comprehensive Approach to Modeling, Characterizing and Optimizing for Metastability in FPGAs ................................................................. 167
  Doris Chen, Deslanand Singh, Jeffrey Chromczak, David Lewis, Ryan Fung, David Neto, Vaughn Betz (Altera Corporation)

• Variation-Aware Placement for FPGAs with Multi-cycle Statistical Timing Analysis ................................................................. 177
  Gregory Lucas, Chen Dong, Deming Chen (University of Illinois Urbana-Champaign)

• Global Delay Optimization Using Structural Choices ..................................... 181
  Alan Mishchenko, Robert Brayton (University of California, Berkeley), Stephen Jang (non-affiliated)

• Building a Faster Boolean Matcher Using Bloom Filter .................................. 185
  Chun Zhang (Fudan University), Yu Hu (University of Alberta), Lingli Wang (Fudan University), Lei He (University of California, Los Angeles), Jiarong Tong (Fudan University)

Session 6: High-Performance Applications

• Haptic Rendering of Deformable Objects Using a Multiple FPGA Parallel Computing Architecture ................................................................. 189
  Behzad Mahdavikiah, Ramin Mafi, Shahin Sirouspour, Nicola Nicolici (McMaster University)

• A 1 Cycle-Per-Byte XML Parsing Accelerator ............................................. 199
  Zefu Dai, Nick Ni, Jianwen Zhu (University of Toronto)

• A Modular NFA Architecture for Regular Expression Matching ..................... 209
  Hao Wang, Shi Pu, Gabriel Knezek, Jyh-Charn Liu (Texas A&M University)

• Scalable Network Virtualization Using FPGAs ............................................. 219
  Deepak Umiikrishnan, Ramakrishna Vadlamani, Yong Liao, Abhishek Dwaraki (University of Massachusetts, Amherst), Jérémie Crenne (European University of Brittany), Lixin Gao, Russell Tessier (University of Massachusetts, Amherst)
Session 7: Reliability

- **Degradation in FPGAs: Measurement and Modelling** ................................................................. 229
  Edward A. Stott, Justin S. J. Wong, Pete Sedcole, Peter Y. K. Cheung (Imperial College London)
- **On-Line Sensing for Healthier FPGA Systems** ................................................................. 239
  Kenneth M. Zick, John P. Hayes (University of Michigan)
- **Voter Insertion Algorithms for FPGA Designs Using Triple Modular Redundancy** .......... 249
  Jonathan M. Johnson, Michael J. Wirthlin (Brigham Young University)
- **Maximizing Area-Constrained Partial Fault Tolerance in Reconfigurable Logic** .......... 259
  David L. Foster (Kettering University), Darrin M. Hanna (Oakland University)

Session 8: Architecture

- **The Impact of Interconnect Architecture on Via-Programmed Structured ASICs (VPSAs)** ................................................................. 263
  Usman Ahmed, Guy G. F. Lemieux, Steven J. E. Wilton (University of British Columbia)
- **Efficient FPGAs Using Nanoelectromechanical Relays** ...................................................... 273
  Chen Chen, Roozbeh Parsa, Nishant Patil, Soogine Chong, Kerem Akarvardar, J Provine (Stanford University),
  David Lewis, Jeff Watt (Altera Corporation),
  Roger T. Howe, H.-S. Philip Wong, Subhasish Mitra (Stanford University)

Poster Session 1: Applications

- **A Multi-FPGA Based Platform for Emulating a 100M-transistor-scale Processor with High-speed Peripherals** ................................................................. 283
  Huandong Wang, Xiang Gao, Yunji Chen, Dan Tang, Weiwu Hu (Chinese Academy of Sciences)
- **Towards 5ps Resolution TDC on a Dynamically Reconfigurable FPGA** ........................................ 283
  Marc-Andre Daigneault, Jean Pierre David (École Polytechnique de Montréal)
- **An Architecture for Graphics Processing in an FPGA** ...................................................... 283
  Marcus Dutton, David Keezer (Georgia Institute of Technology)
- **FPGA Implementation of Highly Parallelized Decoder Logic for Network Coding** ........ 284
  Sunwoo Kim, Won W. Ro (Yonsei University)
- **Application of a Reconfigurable Computing Cluster to Ultra High Throughput Genome Resequeing** ................................................................. 284
  Kristian Stevens (University of California, Davis), Henry Chen, Terry Filiba (Berkeley Wireless Research Center),
  Peter McMahon (Stanford University), Yun S. Song (University of California, Berkeley)
- **FPGA Based Chip Emulation System for Test Development and Verification of Analog and Mixed Signal Circuits** ................................................................. 284
  Rahul Bhattacharya (IIT Kharagpur), Santosh Biswas (IIT Guwahati), Siddhartha Mukhopadhyay (IIT Kharagpur)
- **LambdaRank Acceleration for Relevance Ranking in Web Search Engines** ...................... 285
  Jing Yan, Ning-Yi Xu, Xiong-Fei Cai, Rui Gao (Microsoft Research Asia),
  Yu Wang, Rong Luo (Tsinghua University), Feng-Hsiung Hsu (Microsoft Research Asia)
- **Memory Efficient String Matching: A Modular Approach on FPGAs** ........................................ 285
  Hoang Le, Yi-Hua Yang, Viktor K. Prasanna (University of Southern California)
- **Implementing Dynamic Information Flow Tracking on Microprocessors with Integrated FPGA Fabric** ................................................................. 285
  Skyler Schneider, Daniel Y. Deng, Daniel Lo, Greg Malysa, G. Edward Suh (Cornell University)

Poster Session 2: High-Level Abstractions & CAD Tools

- **A Semi-Automatic Toolchain for Reconfigurable Multiprocessor Systems-on-Chip: Architecture Development and Application Partitioning** ................................................................. 286
  Diana Goehringer (Fraunhofer IOSB), Michael Huebner (Karlsruher Institute of Technology),
  Michael Benz (Fraunhofer IOSB), Juergen Becker (Karlsruher Institute of Technology)
- **A Dependency Graph Based Methodology for Parallelizing HLL Applications on FPGA** .... 286
  Sunita Chandrasekaran, Shilpa Shenbagh, Douglas L. Maskell (Nanyang Technological University)
• Design Space Exploration of Throughput-Optimized Arrays from Recurrence Abstractions ........................................... 286
  Arpith C. Jacob, Jeremy D. Buhler, Roger D. Chamberlain (Washington University in St. Louis)

• Reconfigurable Custom Floating-Point Instructions .......................................................... 287
  Zhanpeng Jin (University of Pittsburgh), Richard Neil Pittman, Alessandro Forin (Microsoft Research)

• Multiplier Architectures for FPGA Double Precision Functions ........................................... 287
  Y Hamid, Martin Langhammer (Altera Corporation)

• Automatic Tool Flow for Shift-Register-LUT Reconfiguration: Making Run-Time Reconfiguration Fast and Easy ........................................... 287
  Brahim Al Farisi, Karel Bruncel, Harald Devos, Dirk Stroobandt (Ghent University)

• Odin II - An Open-source Verilog HDL Synthesis Tool for FPGA CAD Flows .................. 288
  Peter A. Jamieson (Miami University), Keneth B. Kent (University of New Brunswick)

• LUT-Based FPGA Technology Mapping for Reliability ................................................... 288
  Jason Cong (University of California, Los Angeles), Kirli Minkovich (University of California, Los Angeles)

• Aggressive Overclocking Support using a Novel Timing Error Recovery Technique on FPGAs ........................................... 288
  Amir Masoud Gharahbaghi, Bijan Alizadeh, Masahiro Fujita (University of Tokyo)

• A Heuristic Algorithm for LUT-based FPGA Technology Mapping Using the Lower Bound for DAG Covering Problem ........................................... 289
  Taiga Takata, Yusuke Matsunaga (Kyushu University)

Poster Session 3: Architecture & Design Studies

• Heterogeneous-ASIF: An Application Specific Inflexible FPGA Using Heterogeneous Logic Blocks ........................................... 290
  Husain Parvez, Zied Marrakchi, Habib Mehrez (Université Pierre et Marie Curie)

• Scalable Architecture for Programmable Quantum Gate Array ........................................... 290
  Mingjie Lin, Yaling Ma (University of California, Berkeley)

• Fine-Grained vs. Coarse-Grained Shift-and-Add Arithmetic in FPGAs ........................ 290
  Julien Lamoureux, Scott Miller, Mihini Sima (University of Victoria)

• DRAM-Based FPGA Enabled by Three-Dimensional (3D) Memory Stacking ................ 290
  Yangyang Pan, Tong Zhang (Rensselaer Polytechnic Institute)

• Modeling and Simulation of Nano Quantum FPGAs .................................................... 291
  Mohammed Niamat, Somvya Paruganti, Tejas Raviraj (University of Toledo)

• Nano-Magnetic Non-Volatile CMOS Circuits for Nano-Scale FPGAs ........................... 291
  Larkinhoon Lems, James A. Weaver, Metha Jeeadrit, James S. Harris (Stanford University)

• High-performance FPGA Based on Novel DSS-MOSFET and Non-volatile Configuration Memory ........................................... 291
  Shinichi Yasuda, Tetsufumi Tanamoto, Kazutaka Ikegami, Atsushi Kinoohita, Keiko Abe, Hirotsuka Nishino, Shinobu Fujita (Toshiba Corporation)

• Design and Evaluation of a Parameterizable NoC Router for FPGAs ............................. 292
  Mike Brugge, Mohammed A. S. Khalid (University of Windsor)

• Energy Reduction with Run-Time Partial Reconfiguration .............................................. 292
  Shaoshan Liu (University of California, Irvine), Richard Neil Pittman, Alessandro Forin (Microsoft Research)

• Minimizing Partial Reconfiguration Overhead with Fully Streaming DMA Engines and Intelligent ICAP Controller ........................................... 292
  Shaoshan Liu (University of California, Irvine), Richard Neil Pittman, Alessandro Forin (Microsoft Research)

• FPGA-Based Prototyping of a 2D MESH / TORUS On-Chip Interconnect ....................... 293
  Donglai Dai, Arinriddha Vaidya, Roy Saharoy, Seungjoon Park, Dongkook Park, Hariharan L. Thantry, Ralf Plate, Elmar Maas, Akihlesh Kumar, Mani Azimi (Intel Corporation)

Author Index .......................................................................................................................... 295