2009 International Symposium on System-on-Chip

(SOC 2009)

Tampere, Finland
5 – 7 October 2009

Editors:

Jari Nurmi
Jarmo Takala
Olli Vainio

IEEE Catalog Number: CFP09554-PRT
SoC Symposium 2009 Technical Papers

Simultaneous PVT-tolerant voltage-island formation and core placement for thousand-core platforms
Sohaib Majzoub, Resve Saleh, Steve Wilton, and Rabab Ward
University of British Columbia, Canada

Fault-tolerant communication over micronmesh NOC with micron-message passing protocol
Heikki Karinlahti and Jari Nurmi
Tampere University of Technology, Finland

Adaptive circuit block model for power supply noise analysis of low power system-on-chip
Matthias Eireiner¹, Paul Wallner², Andreas Schoene², Stephan Henzler², Ulrich Fiedler³, and Doris Schmitt-Landsiedel²
¹Technical University Munich, Germany, ²Infineon Technologies AG, Germany

Parameterizing simulated annealing for distributing Kahn process networks on multiprocessor SoCs
Heikki Orsila, Erno Salminen, and Timo Hämäläinen
Tampere University of Technology, Finland

Energy and bandwidth aware mapping of IPs onto regular NoC architectures using multi-objective genetic algorithms
Kshitij Bhardwaj¹ and Rabindra Jena²
¹DAVV, India, ²Institute of Management & Technology, India

Physical realization oriented area-power-delay tradeoff exploration
Volker Gieren¹, Christian Pantis, and Jari Nurmi²
¹Catena Radio Design bv, the Netherlands, ²Tampere University of Technology, Finland

Diagnosis of faults in template-based asynchronous circuits
Behnam Ghavami¹, Hamid-Reza Zarandi¹, Arezoo Salarpour², and Hossein Pedram¹
¹Amirkabir University of Technology, Iran, ²University of Science and Technology, Iran

Dynamic workload peak detection for slack management
Aleksandar Milutinovic¹, Kees Goossens², and Gerard J.M. Smit²
¹University of Twente, the Netherlands, ²NXP Semiconductors & Delft University of Technology, the Netherlands

Building asynchronous routers with independent sub-channels
Wei Song and Doug Edwards
the University of Manchester, UK

Soft NMR: Exploiting statistics for energy-efficiency
Eric Kim, Rami Abdallah, and Naresh Shanbhag
University of Illinois at Urbana Champaign, USA

Performance analysis of LTE protocol processing on an ARM based mobile platform
David Szczesny¹, Anas Showk², Sebastian Hess², Uwe Hildebrand², Valerio Frascolla², and Attila Bilgic³
¹Ruhr-Universität Bochum, Germany, ²Comneon GmbH, Germany

Performance modeling of parallel applications on MPSoCs
Marco Lattuada, Christian Pilato, Antonino Tumeo, and Fabrizio Ferrandi
Politecnico di Milano, Italy

Impact of device variability in the communication structures for future synchronous SoC designs
Faiz ul Hassan, Binjie Cheng, Wim Vanderbauwhede, and Fernando Rodriguez
University of Glasgow, UK

Flexible DOR routing for virtualization of multicore chips
Frank Olaf Sem-Jacobsen¹, Tor Skeie¹, Samuel Rodrigo², José Flich², Davide Bertozzi³, and Simone Medardoni³
¹Simula Research Laboratory, Norway, ²Technical University of Valencia, Spain, ³University of Ferrara, Ferrara, Italy
Automatic generation of memory interfaces ......................................................... 77
David Kammler¹, Bastian Bauwens¹, Ernst Martin Wittel¹, Gerd Ascheid¹, Rainer Leupers¹, Heinrich Meyr¹, Anupam Chattopadhyay¹
¹RWTH Aachen University, Germany, ²CoWare India Private Ltd., India

Two phase clocked adiabatic static CMOS logic .................................................. 83
Nazrul Anuar Nayan, Yasuhiro Takahashi, and Toshikazu Sekine
Gifu University, Japan

Evaluation of static and dynamic task mapping algorithms in NoC-based MPSoCs .......... 87
Ewerson Carvalho, César Marcon, Ney Calazans, and Fernando Moraes
Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

Minimizing area costs in GPS applications on a programmable DSP by code compression ... 91
Pita Saastamoinen¹, Jari Nurmi¹, Ilkka Saastamoinen¹, and Mikko Laiho²
¹Tampere University of Technology, Finland, ²Atheros Communications, Finland

Scheduling framework for real-time dependable NoC-Based systems ......................... 95
Mihkel Tagel, Peeter Ellerree, and Gert Jervan
Tallinn University of Technology, Estonia

Yield-oriented evaluation methodology of networks-on-chip routing implementations ........ 100
Samuel Rodríguez¹, Carles Hernández¹, José Flich¹, Federico Silla¹, José Dutó¹, Simone Medardoni¹, Davide Bertozzi¹, Andreu Mejía¹, and Dongglai Dai¹
¹Universidad Politécnica de Valencia, Spain, ²University of Ferrara, Italy, ³Intel

A Multi-core signal processor for heterogeneous reconfigurable computing ............... 106
Davide Rossi¹, Fabio Campi², Antonio Deledda², Claudio Mucci², Stefano Pucillo², Sean Whitty³, Rolf Ernst³, Stéphane Chevobbe⁴, Stephane Guyetand⁴, Matthias Kühnle⁴, Michael Hübscher⁴, Jürgen Becker⁴, and Wolfram Putzke-Roeming⁶
¹University Of Bologna, Italy, ²STMicroelectronics, Italy, ³Technische Universität Braunschweig, Germany, ⁴CEA, France, ⁵University Of Karlsruhe, Germany, ⁶Thomson, Germany

RTL-to-layout implementation of an embedded coarse grained architecture for dynamically reconfigurable computing in systems-on-chip ........................................... 110
Fabio Campi¹, Ralf König², Michael Dreschmann², Moritz Neukirchner², Damien Picard², Michael Jüttner², Eberhard Schlüter², Antonio Deledda⁴, Davide Rossi⁴, Alberto Pasini⁴, Michael Hübscher⁴, Jürgen Becker⁴, and Roberto Guerrieri⁴
¹STMicroelectronics, Italy, ²University of Karlsruhe, Germany, ³Technical University of Braunschweig, Germany, ⁴Université de Bretagne Occidentale, France, ⁵Technical University of Chemnitz, Germany, ⁶PACT XPP Technologies, Germany, ⁷University of Bologna, Italy

Analysis of memory access optimization for motion compensation frames in MPEG-4 .......... 114
Haitham Habi¹, Johan Ersfolk², Johan Lilius²
¹Åbo Akademi University, Finland, ²TUCS and Åbo Akademi University, Finland

Pathfinding: A design methodology for fast exploration and optimization of 3D-stacked integrated circuits ........................................................................... 118
Dragomir Milojević¹, Riko Radojičić², Roger Carpenter², and Pol Marchal²
¹ULB, Belgium, ²Qualcomm, USA, ³Javelin DA, USA, ⁴IMEC, Belgium

Multi-compartment: A new architecture for secure co-hosting on SoC ....................... 124
Joël Porquet¹, Christian Schwarz², and Alain Greiner²
¹STMicroelectronics, France, ²UPMC/LIP6, France

Performance analysis of multi-channel memories in mobile devices ......................... 128
Jari Nikara, Eero Aho, Petri Tuominen, and Kimmo Kiulinen
Nokia Research Center, Finland

System architecture for 3GPP LTE modem using a programmable baseband processor .... 132
Johan Eilert, Di Wu, and Dake Liu
Linköping University, Sweden

On the performance of 3GPP LTE baseband using SB3500 ..................................... 138
Zhenyu Tu, Meng Yu, Daniel Iancu, Mayan Moudgill, and John Glossner
Sandbridge Technologies Inc., USA