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ISQED 2010 – Table of Contents

1A: SRAM Manufacturability
Chair: Saraju Mohanty - Univ of North Texas; Co-Chair: Valeriy Sukharev - Mentor Graphics

1A.1: Limits of Bias Based Assist Methods in Nano-Scale 6T SRAM .................................................................................................................................................. 1
Randy W. Mann, Satyanand Nalam, Jiajing Wang, Benton H. Calhoun – University of Virginia

1A.2: Variability Resilient Low-power 7T-SRAM Design for nano-Scaled Technologies .......................................................................................................................................................................................... 9
Touqeer Azam, Binjie Cheng, David R.S. Cumming – University of Glasgow

1A.3: Robust Importance Sampling for Efficient SRAM Yield Analysis .......................................................................................................................................................................................... 15
Takanori Date, Shiho Hagiwara, Kazuya Masu – Tokyo Institute of Technology; Takashi Sato – Kyoto Univ*

1A.4: An Accurate Modeling Method Utilizing Application Specific Statistical Information and Its Application to SRAM Yield Estimation .......................................................................................................................................................................................... 22
Hidetoshi Matsuoka, Hiroshi Ikeda, Hiroyuki Hibuchi, Yoshinori Tomita – Fujitsu Microelectronics Ltd

1B: Mixed Signal and Power Control Circuits
Chairs: Syed Alam, Mark Budnik

1B.1: Adaptive Power Gating for Function Units in a Microprocessor .......................................................................................................................................................................................... 29
Kimiyoshi Usami, Tatsunori Hashida, Satoshi Koyama, Tatsuya Yamamoto – Shibaura Inst of Technology; Daisuke Ikebuchi, Hideharu Amano – Keio Univ; Mitaro Namiki – Tokyo Univ of Agriculture & Technology; Masaaki Kondo – The University of Electro-Communications; Hiroshi Nakamura – University of Tokyo

1B.2: A Dual-Level Adaptive Supply Voltage System for Variation Resilience .......................................................................................................................................................................................... 38
Kyu-Nam Shim, Jiang Hu, Jose Silva-Martinez – Texas A&M University

1B.3: A Low Power Charge Redistribution ADC With Reduced Capacitor Array .......................................................................................................................................................................................... 44
Mallik Kandala, Ramgopal Sekar, Chenglong Zhang, Haibo Wang – Southern Illinois Univ-Carbondale

1B.4: Leakage Current Analysis for Intra-Chip Wireless Interconnects .......................................................................................................................................................................................... 49
Ankit More and Baris Taskin – Drexel University

1C: Guaranteeing Timing Performance
Chairs: James Lei, Prof. Fujita

1C.1: Toward Effective Utilization of Timing Exceptions in Design Optimization .......................................................................................................................................................................................... 54
Kwangok Jeong, Andrew B. Kahng, Seokhyeong Kang – UC. San Diego

1C.2: Useful Clock Skew Optimization Under a Multi-Corner Multi-Code Design Framework .......................................................................................................................................................................................... 62
Weixiang Shen, Yici Cai, Yongqiang Lu, Qiang Zhou – Tsinghua University
Wei Chen – Magma Design Automation Inc.; Jiang Hu – Texas A&M University*

1C.3: Clock Buffer Polarity Assignment Considering the Effect of Delay Variations .......................................................................................................................................................................................... 69
Minseok Kang and Taewhan Kim – Seoul National University

1C.4: Linear Time Calculation of State-Dependent Power Distribution Network Capacitance .......................................................................................................................................................................................... 75
Shiho Hagiwara, Koh Yamanaga, Kazuya Masu – Tokyo Institute of Technology; Ryo Takahashi -- The University of Tokyo; Takashi Sato -- Kyoto University

1D: Analog Design For Reliability
Chairs: Srinivas Bodapati, Payman Zarkesh-Ha

1D.1: Implementing Self-Testing and Self-Repairing Analog Circuits on Field Programmable Analog Array .......................................................................................................................................................................................... 81
Venkata Naresh Mudireddy, Saravanan Ramamoorthy, Haibo Wang – Southern Illinois Univ Carbondale

1D.2: BSIM4-Based Lateral Diode Model for LNA Co-Designed with ESD Protection Circuit .......................................................................................................................................................................................... 87
Ming-Ta Yang, Yang Du, Charles Teng, Tony Chang, Eugene Worley, Ken Liao, You-Wen Yau and Geoffrey Yeap – Qualcomm

1D.3: Hot Carrier Effects on CMOS Phase-Locked Loop Frequency Synthesizers .......................................................................................................................................................................................... 92
Yang Liu and Ashok Srivastava – Louisiana State University Baton Rouge

1D.4: A Novel All Digital Fractional-N Frequency Synthesizer Architecture with Fast Acquisition and Low Spur .......................................................................................................................................................................................... 99
Jun Zhao and Yong-Bin Kim – Northeastern University

xiii
# 2A: Lithography & Manufacturing

**Chairs:** Fedor Pikus, Valeriy Sukharev

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>2A.1</td>
<td>Photomasks and the Enablement of Circuit Design Complexity</td>
<td>Peter Buck, Franklin Kalk, Craig West – Toppan Photomasks, Inc</td>
</tr>
<tr>
<td>2A.2</td>
<td>High Performance Source Optimization using a Gradient-Based Method in Optical Lithography</td>
<td>Yao Peng, Jinyu Zhang, Yan Wang, Zhiping Yu – Tsinghua University</td>
</tr>
<tr>
<td>2A.4</td>
<td>Assessing Chip-Level Impact of Double-Patterning Lithography</td>
<td>Kwangok Jeong, Andrew Kahng – University of California San Diego; Rasit Topaloglu – GlobalFoundries*</td>
</tr>
</tbody>
</table>

# 2B: Power Aware Memory Design

**Chairs:** Dinesh Somasekhar, Jeffrey Fan

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>2B.1</td>
<td>A 2-Port 6T SRAM Bitcell Design with Multi-Port Capabilities at Reduced Area Overhead</td>
<td>Jawar Singh, Dhiraj Pradhan – University of Bristol; D.S. Aswar – India Dept of Telecommunication; S.P. Mohanty – University of North Texas USA*</td>
</tr>
<tr>
<td>2B.2</td>
<td>Asymmetric 6T SRAM with Two-phase Write and Split Bitline Differential Sensing for Low Voltage Operation</td>
<td>Satyanand Nalam, Benton Calhoun – University of Virginia; Vikas Chandra, Cezary Pietrzyk, Robert Aitken – ARM*</td>
</tr>
<tr>
<td>2B.3</td>
<td>A Robust and Low Power Dual Data Rate (DDR) Flip-Flop Using C-Elements</td>
<td>Srikanth V. Devarapalli, Payman Zarkesh-Ha, and Steven C. Sudharth – University of New Mexico</td>
</tr>
<tr>
<td>2B.4</td>
<td>Optimizing Power and Throughput for M-Out-Of-N Encoded Asynchronous Circuits</td>
<td>Jun Xu, Ge Zhang, Weiwu Hu – Chinese Academy of Sciences; Ge Zhang, Weiwu Hu – Loogson Technology Corporation Limited*</td>
</tr>
</tbody>
</table>

# 2D: Poster Session 1

**Chairs:** Kamesh Gadepally, Lalitha Immaneni

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D.1</td>
<td>Simultaneous Extraction of Effective Gate Length and Low-field Mobility in Non-uniform Devices</td>
<td>Vivek Joshi, Dennis Sylvester – University of Michigan; Kanak Agarwal, IBM Corp.</td>
</tr>
<tr>
<td>2D.2</td>
<td>Statistical Static Timing Analysis Flow for Transistor Level Macros in a Microprocessor</td>
<td>Vivek Nandakumar, Malgorzata Marek-Sadowska – University of California Santa Barbara; David Newmark, Yaping Zhan – Advanced Micro Devices Inc</td>
</tr>
<tr>
<td>2D.4</td>
<td>P3 (Power-Performance-Process) Optimization of Nano-CMOS SRAM using Statistical DOE-ILP</td>
<td>Garima Thakral, Saraju Mohanty, Dhruva Ghai – University of North Texas; Dhiraj Pradhan – University of Bristol*</td>
</tr>
<tr>
<td>2D.5</td>
<td>A Yield Improvement Methodology Based on Logic Redundant Repair with a Repairable Scan Flip-Flop Designed by Push Rule</td>
<td>Masanori Kurimoto, Jun Matsushima, Shigeki Ohbayashi, Yoshiaki Fukui, Michio Komoda and Nobuhiro Tsuda – Renesas Technology Corp.</td>
</tr>
<tr>
<td>2D.6</td>
<td>A Fault-tolerant Structure for Reliable Multi-core Systems Based on Hardware-Software Co-design</td>
<td>Bingbing Xia, Fei Qiao, Huazhong Yang, Hui Wang – Tsinghua University</td>
</tr>
<tr>
<td>2D.7</td>
<td>&quot;Condition-based&quot; Dummy Fill Insertion Method Based on ECP and CMP Predictive Models</td>
<td>Izumi Nitta, Yuji Kanazawa, Daisuke Fukuda, Toshiyuki Shibuya, Naoki Idani, Masaru Ito, Osamu Yamasaki, Norihiro Harada, Takanori Hiramoto – Fujitsu</td>
</tr>
<tr>
<td>2D.9</td>
<td>On the Design of Different Concurrent EDC Schemes for S-Box and GF(p)</td>
<td>Jimson Mathew, Hafizur Rahaman, Dhiraj Pradhan – University of Bristol; Abusaleh Jabir – Oxford Brookes University; Saraju Mohanty – Univ of North Texas*</td>
</tr>
</tbody>
</table>
2D.11: Soft Error Rate Determination for Nanoscale Sequential Logic
Fan Wang – Juniper Network Inc.; Vishwani Agrawal – Auburn University

2D.12: Ultra Low-voltage, Rail-to-Rail Input/Output Stage Operational Transconductance Amplifier (OTA) with High Linearity and its Application in a Gm-C filter
Farzan Rezaei and Seyed Javad Azhari – Iran University of Science and Technology (IUST)

2D.13: A Novel Two-Dimensional Scan-Control Scheme for Test-Cost Reduction
Chia-Yi Lin and Hung-Ming Chen – National Chiao Tung University

2D.14: Accelerating Trace Computation in Post-Silicon Debug
Johnny Kuan, Steven Wilton, Tor Aamodt – University of British Columbia

2D.15: Structural Fault Collapsing by Superposition of BDDs for Test Generation in Digital Circuits
Raimund Ubar, Dmitri Mironov, Jaan Raik, Artur Jutman – Tallinn University of Technology

2D.16: A Novel Probabilistic SET Propagation Method
Sreenivas Gangadhar and Spyros Tragoudas – Southern Illinois University Carbondale

2D.17: Formal Verification of Full-Wave Rectifier using SPICE Circuit Simulation Traces
Kusum Lata and H S Jamadagni – Indian Institute of Science Bangalore

2D.18: OBT Implementation on an OTA-C Band-pass Filter
Pablo Petraschin – Universidad Católica de Córdoba;
Gabriela Peretti, Eduardo Romero – Universidad Tecnologica Nacional

2D.19: Fast Block-iterative Domain Decomposition Algorithm for IR Drop Analysis in Large Power Grid
Yu Zhong and Martin D. F. Wong – University of Illinois at Urbana Champaign

2D.20: ANon-Parametric Approach to Behavioral Device Modeling
Dragoljub (Gagi) Drmanac, Brendon Bolin, Li-C. Wang – UCSB

3A: Variability: Design, Test, and Characterization
Chairs: Peter O'Shea, Narendra Devta-Prasanna

3A.1: Robust Gate Sizing by Uncertainty Second Order Cone
Jin Sun and Janet Wang – The University of Arizona

3A.2: Is Built-In Logic Redundancy Ready for Prime Time?
Chris Allsup – Synopsys Inc.

3A.3: Variation-Aware Speed Binning of Multi-core Processors
John Sartori and Rakesh Kumar – University of Illinois at Urbana Champaign
Ashish Pant and Puneet Gupta – UCLA

3A.4: Use of Scalable Parametric Measurement Macro to Improve Semiconductor Technology Characterization and Product Test
Jeanne Bickford, Nazmul Habib, John Goss, Robert McMahon, Rajiv Joshi, Rouwaida Kanj – IBM

3A.5: Accurate Multi-Specification DPPM Estimation Using Layered Sampling Based Simulation
Ender Yilmaz – Arizona State University

3B: Emerging Device and Design Techniques
Chairs: Paul Tong, Bao Liu

3B.1: Scalability of PCMO-based Resistive Switch Device in DSM Technologies
Yiran Chen, Wei Tian, Xiaobin Wang, Wenzhong Zhu – Seagate Technology LLC
Hai Li – Polytechnic Institute of NYU

3B.2: A Low Power System with Adaptive Data Compression for Wireless Monitoring of Physiological Signals and its Application to Wireless Electroencephalography
Jeremy Tolbert, Pratik Kabali, Simeranjit Brar, Saiibal Mukhopadhyya – Georgia Institute of Technology

3B.3: Modeling and Analysis of III-V Logic FETs for Devices and Circuits: Sub-22nm Technology III-V SRAM Cell Design
Saeroounter Oh, Jeongha Park, S. Simon Wong, H.-S. Philip Wong – Stanford University

3B.4: Die-level Leakage Power Analysis of FinFET Circuits Considering Process Variations
Prateek Mishra, Ajay Bhoj, Niraj Jha – Princeton University

3B.5: Using Time-Aware Memory Sensing to Address Resistance Drift Issue in Multi-Level Phase Change Memory
Wei Xu and Tong Zhang – Rensselaer Polytechnic Institute
3C: Power and Performance Issues in System-Level Design
Chairs: Lech Jóźwiak, Rajesh Berigei

3C.1: Minimizing the Power Consumption of a Chip Multiprocessor System under an Average Throughput Constraint
Mohammad Ghasemazar, Ehsan Pakbaznia, Massoud Pedram – University of Southern California

Yang Liu – Juniper Networks; Jibang Liu, Tong Zhang – Rensselaer Polytechnic Institute

3C.3: Quality-driven Methodology for Demanding Accelerator Design
Lech Jóźwiak and Yahya Jan – Eindhoven University of Technology

3C.4: Thermal-Aware Job Allocation and Scheduling for Three Dimensional Chip Multiprocessor
Shaobo Liu, Jingyi Zhang, Qing Wu, Qinnru Qiu – State University of New York at Binghamton

3C.5: Thermal-Aware Lifetime Reliability in Multicore Systems
Shengquan Wang – University of Michigan-Dearborn; Jian-Jia Chen – ETH Zurich

3D: Poster Session 2
Chairs: Kamesh Gadepally, Lalitha Immaneni

3D.1: A Comprehensive Model for Gate Delay under Process Variation and Different Driving and Loading Conditions
Mingzhi Gao, Zuocang Ye, Yao Peng, Yan Wang, Zhiping Yu – Tsinghua University

3D.2: Skew Analysis and Bounded Skew Constraint Methodology for Rotary Clocking Technology
Vinayak Honkote and Baris Taskin – Drexel University

3D.3: A MATLAB-Based Technique for Defect Level Estimation Using Data Mining of Test Fallout Data versus Fault Coverage
Kanad Chakraborty – Cypress Semiconductor

3D.4: Constraint Analysis and Debugging for Multi-Million Instance SoC Designs
Long Fei, Loa Mize, Cho Moon, Bill Mullen, Sonia Singhal – Synopsys Inc

3D.5: Variation Aware Guard-Banding For SOC Static Timing Analysis

3D.6: Asymmetric Issues of FinFET Device after Hot Carrier Injection and Impact on Digital and Analog Circuits
Chenyue Ma, Hao Wang, Xiufang Zhang, Frank He, Yadong He, Xing Zhang, Xinnan Lin – Peking Univ

3D.7: A Novel Low Voltage Current Compensated High Performance Current Mirror/NIC
Khalil Monfaredi, Hassan Faraji Baghtash, Seyed Javad Azhari – Iran University of Science and Technology (IUST)

3D.8: Domino Gate with Modified Voltage Keeper
Jinhui Wang, Wuchen Wu, Ligang Hou – Beijing University of Technology; Na Gong – State University of New York at Buffalo

3D.9: Leakage Temperature Dependency Modeling in System Level Analysis
Huang Huang, Gang Quan, Jeffrey Fan – Florida International University

3D.10: Process Variation Tolerant On-Chip Communication Using Receiver and Driver Reconfiguration
Ethiopia Nigussie, Juha Plosila, Jouni Isoaho – University of Turku

Basab Datta and Wayne Burleson – University of Massachusetts-Amherst

3D.12: New SRAM Design Using Body Bias Technique for Ultra Low Power Applications
Fasrhad Moradi, Dag Wilsland, Yngvar Berg, Tuan Vu Cao – University of Oslo; Hamid Mahmoodi – SanFrancisco State University; Fasrhad Moradi – Purdue University

3D.13: Body Bias Driven Design Synthesis for Optimum Performance per Area
Maurice Meijer and Jose Pineda de Gyvez – NXP Semiconductors

3D.14: Methodology to Ensure Circuit Robustness and Exceptional Silicon Quality while Proliferating Designs Across Process Revisions with High Productivity
Nitin Srimal – intsys

3D.15: A Multilevel Multilayer Partitioning Algorithm For Three Dimensional Integrated Circuits
Yu Cheng Hu, Yin Lin Chung, Mely Chen Chi – Chung Yuan Christian University

3D.16: Low Power Clock Gates Optimization For Clock Tree Distribution
Slong Kiong Teng – Intel Microelectronics; Dr Norhayati Soin – University of Malaya

3D.17: An Innovative Method to Automate the Waiver of IP-Level DRC Violations
John Ferguson, Sandeep Koranne, David Abercrombie – Mentor Graphics
3D.18: Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Alex Veidenbaum, Fadi Kurdahi – UC-Irvine

3D.19: Antenna Violation Avoidance/Fixing for X-Clock Routing
Chia-Chun Tsai – Nanhua University;
Chung-Chieh Kuo, Lin-Jeng Gu, Trong-Yen Lee – National Taipei University of Technology

Masahiro Fujita, Hideo Tanida, Tasuku Nishihara, Takeshi Matsumoto – University of Tokyo;
Fei Gao – Fujitsu, Ltd.

3D.21: Level Matrix Propagation for Reliability Analysis of Nano-scale Circuits based on Probabilistic Transfer Matrix
Hicham Ezzat and Lirida Naviner – Télécom ParisTech; Hicham Ezzat – Université Française d’Egypte

3D.22: The Design of a Low-Power Low-Noise Phase Lock Loop
Abishek Mann, Amit Karalkar, Lili He, Morris Jones – San Jose State University

3D.23: Novel Low-Power 12-bit SAR ADC for RFID Tags
Daniela De Venuto – Politecnico di Bari; Eduard Stikvoort;
David Castro, Youri Ponomarev – NXP Semiconductors

3D.24: Adaptive Task Allocation for Multiprocessor SoCs in Real-Time Energy Harvesting Systems
Tongquan Wei – East China Normal University;
Yonghe Guo, Xiaodao Chen, Shiyian Hu – Michigan Technological University*

3D.25: Multi-Programming Environment for Structure Under Pads (SUP) and Via Arrays Pattern Recognition Automated Classification System
Suraya Mohd Yusof and Lau Meng Tee – National Semiconductor Sdn.Bhd

4A: Parametric and Delay Test
Chairs: Srivatsa Vasudevan, Ramyanshu Datta

4A.1: Real-Time Adaptive Hybrid BIST Solution for Very-Low-Cost ATE Production Testing of A/D Converters with Optimal DPPM
Sachin D. Dasnurkar and Jacob A. Abraham – University of Texas at Austin

4A.2: On Evaluating Speed Path Detection of Structural Tests
Jing Zeng, Jing Wang, Chia-Ying Chen, Michael Mateja – AMD; Li-C. Wang – UC Santa Barbara

4A.3: Slack-Based Approach for Peak Power Reduction during Transition Fault Testing
Manu Baby and Vijay Sarathi – Dubai Circuit Design DSO

4A.4: Case Studies of Mixed-Signal DFT
Ramyanshu Datta, Mahit Warhadpande, Dale Heaton, S Aarthi, Ram Jonnavithula – Texas Instruments Inc

4B: PDI
Chairs: Lalitha Immaneni, Kamesh Gadepally

4B.1: Efficient Hierarchical Discretization of Off-chip Power Delivery Network Geometries for 2.5D Electrical Analysis
Mosin Mondal, James Pingenot, Vikram Jandhyala – University of Washington

4B.2: Yield Improvement of 3D ICs in the Presence of Defects in Through Signal Vias
Rajeev Nain, Shantesh Pinge, Malgorzata Chrzanowska-Jeske – Portland State University

5A: Advances in Power Distribution, Placement and Routing
Chairs: Shiyan Hu, Vamsi Srikantham

5A.1: A Negotiated Congestion-based Router for Simultaneous Escape Routing
Qiang Ma, Tan Yan, Martin D. F. Wong – University of Illinois at Urbana-Champaign

Nithin S K, Gowryshankar Shanmugham, Sreram Chandrashekar – Texas Instruments

5A.3: Analog Placement and Global Routing Considering Wiring Symmetry
Yu-Ming Yang and Iris Hui-Ru Jiang – National Chiao Tung University

5A.4: Worst-Case Noise Prediction With Non-zero Current Transition Times for Early Power Distribution System Verification
Peng Du, Xiang Hu, Shih-Hung Weng, Amirali Shayan, Chung-Kuan Cheng – University of California San Diego; Xiaoming Chen – Qualcomm Inc.; A. Ege Engin – San Diego State University

5A.5: Fixed Outline Multi-Bend Bus Driven Floorplanning
Wenxu Sheng, Sheqin Dong – Tsinghua University; Yuliang Wu – The Chinese University of Hong Kong; Satoshi Goto – Waseda University*
## 5B: Aging Analysis & Mitigation
Chairs: Srinivas Bodapati, Keith Bowman

| 5B.1: Scalable Methods for the Analysis and Optimization of Gate Oxide Breakdown | Jianxin Fang and Sachin Sapatnekar - University of Minnesota | 638 |
| 5B.2: Comparative Study on Delay Degrading Estimation Due to NBTI with Circuit/Instance/Transistor-Level Stress Probability Consideration | Hiroaki Konoura, Yukio Mitsuyama, Masanori Hashimoto, Takao Onoye - Osaka University | 646 |
| 5B.3: Multi-Corner, Energy-Delay Optimized, NBTI-Aware Flip-Flop Design | Hamed Abrishami, Safar Hatami, Massoud Pedram - University of Southern California | 652 |
| 5B.4: Signal Probability Control for Relieving NBTI in SRAM Cells | Yuji Kunitake, Hiroto Yasuura - Kyushu University; Toshinori Sato - Fukuoka University | 660 |
| 5B.5: Early-Stage Determination of Current-Density Criticality in Interconnects | Goeran Jerke - Robert Bosch GmbH; Jens Lienig - Dresden University of Technology | 667 |

## 5C: Test, Quality, Cost and Debug
Chairs: Priyadarsan Patra, Shankar Hemmady

| 5C.1: Automated Silicon Debug Data Analysis Techniques for a Hardware Data Acquisition Environment | Yu-Shen Yang, Brian Keng, Andreas Veneris - University of Toronto; Nicola Nicolici - McMaster University; Sean Safarpour - Venna Technologies Inc. | 675 |
| 5C.2: Layout-Aware Illinois Scan Design for High Fault Coverage | Shibaji Banerjee, Jimson Mathew, Dhiraj Pradhan - University of Bristol; Saraju P Mohanty - Univ of North Texas - Denton | 683 |
| 5C.3: Multi-Degree Smoother for Low Power Consumption in Single and Multiple Scan-Chains BIST | Abdalatif S. Abu-Issa - Birzeit University; Steven F. Quigley - The University of Birmingham | 689 |
| 5C.4: Multiplexed Trace Signal Selection Using Non-Trivial Implication-Based Correlation | Sandesh Prabhakar and Michael Hsiao - Virginia Tech | 697 |
| 5C.5: Modeling and Verification of Industrial Flash Memories | Sandip Ray - University of Texas at Austin; Jayanta Bhadra, Thomas Portlock, Ronald Syzdek - Freescale Semiconductor Inc. | 705 |

## 5D: System-level NoC, SoC and ASIC design
Chairs: Makram Mansour, Sao-Jie Chen

| 5D.2: UC-PHOTON: A Novel Hybrid Photonic Network-on-Chip for Multiple Use-Case Applications | Shirish Bhirat and Sudeep Pasricha - Colorado State University - Fort Collins | 721 |
| 5D.4: Slack Allocation for Yield Improvement in NoC-based MPSoCs | Brett Meyer, Adam Hartman, Don Thomas - Carnegie Mellon University | 738 |
| 5D.5: Power-Yield optimization in MPSoC Task Scheduling under Process Variation | Mahmoud Mottazpour, Esmaeel Sanaei, Maziar Goudarzi - Sharif University of Technology | 747 |

## 6A: Clocking Strategy for Modern Low Power Multi-Core & Structured ASICs
Chairs: Sanghamitra Roy, Mark Young

<p>| 6A.1: A Revisit to the Primal-Dual Based Clock Skew Scheduling Algorithm | Min Ni - Synopsys Inc.; Seda Ogrenç Memik - Northwestern University | 755 |
| 6A.2: Clock Buffer Polarity Assignment Considering Capacitive Load | Jianchao Lu and Baris Taskin - Drexel University | 756 |
| 6A.3: A Low Power Clock Network Placement Framework | Dawel Liu, Qiang Zhou, Yongqiang Lv, Jinian Bian - Tsinghua University | 771 |</p>
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Authors</th>
<th>Institution</th>
</tr>
</thead>
<tbody>
<tr>
<td>6A.4</td>
<td>Clock Routing for Structured ASICs with Via-Configurable Fabrics</td>
<td>Rung-Bin Lin, I-Wei Lee, Wen-Hao Chen - Yuan Ze University</td>
<td></td>
</tr>
<tr>
<td>6A.5</td>
<td>Analysis of Power Supply Induced Jitter in Actively De-skewed Multi-Core Systems</td>
<td>Derek Chan and Matthew Guthaus - UC Santa Cruz</td>
<td></td>
</tr>
<tr>
<td>6B.1</td>
<td>Analyzing and Minimizing Effects of Temperature Variation and NBTI</td>
<td>Abhishek Sinkar and Nam Sung Kim - University of Wisconsin-Madison</td>
<td></td>
</tr>
<tr>
<td>6B.2</td>
<td>Signal Processing Methods and Hardware-Structure</td>
<td>Minki Cho and Saibal Mukhopadhyay - Georgia Institute of Technology</td>
<td></td>
</tr>
<tr>
<td>6B.3</td>
<td>A Convex Optimization Framework for Leakage-Aware</td>
<td>Sanghamitra Roy and Koushik Chakraborty - Utah State University</td>
<td></td>
</tr>
<tr>
<td>6B.4</td>
<td>Improving the Process Variation Tolerability of Flip-Flops for UDSM Circuit Design</td>
<td>Eun Ju Hwang, Wook Kim, Young Hwan Kim - Pohang University of Science and Technology</td>
<td></td>
</tr>
<tr>
<td>6B.5</td>
<td>Interconnect Delay and Slew Metrics Using the Extreme Value Distribution</td>
<td>Jun-Kuei Zeng and Chung-Ping Chen - National Taiwan University</td>
<td></td>
</tr>
<tr>
<td>6C.1</td>
<td>Design Methodology of Variable Latency Adders with Multistage Function Speculation</td>
<td>Yongpan Liu, Yinan Sun, Yihao Zhu, Huazhong Yang - Tsinghua University</td>
<td></td>
</tr>
<tr>
<td>6C.2</td>
<td>Accurate Statistical Soft Error Rate (SSER) Analysis</td>
<td>Yu-Shin Kuo, Huan-Kai Peng, Charles H.-P. Wen - National Chiao Tung University</td>
<td></td>
</tr>
<tr>
<td>6C.3</td>
<td>Measurement Circuits for Acquiring SET Pulse Width Distribution</td>
<td>Ryo Harada, Yukio Mitsuyama, Masanori Hashimoto, Takao Onoye - Osaka University</td>
<td></td>
</tr>
<tr>
<td>6C.5</td>
<td>Comparative Analysis and Study of Metastability on High-Performance Flip-Flops</td>
<td>David Li, Pierce Chuan, Manoj Sachdev - University of Waterloo</td>
<td></td>
</tr>
<tr>
<td>6D.1</td>
<td>Reliability Analysis of Analog Circuits by Lifetime Yield Prediction</td>
<td>Xin Pan and Helmut Graeb - Technische Universitaet Muenchen</td>
<td></td>
</tr>
<tr>
<td>6D.2</td>
<td>The Compatibility Analysis of Thread Migration and DVFS in Multi-Core Processor</td>
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<td></td>
</tr>
<tr>
<td>6D.3</td>
<td>Analog Behavioral Modeling Flow using Statistical Learning Method</td>
<td>Hui Li, Makram Mansour, Sury Maturi - National Semiconductor; Li Wang - University of California-Santa Barbara</td>
<td></td>
</tr>
<tr>
<td>6D.4</td>
<td>Coprocessor Design Space Exploration Using High Level Synthesis</td>
<td>Avinash Lakshminarayana, Sumit Ahuja, Sandeep Shukla - Virginia Tech</td>
<td></td>
</tr>
<tr>
<td>6D.5</td>
<td>Methodology From Chaos in IC Implementation</td>
<td>Kwangok Jeong and Andrew Kahng - University of California San Diego</td>
<td></td>
</tr>
</tbody>
</table>

6C: Fault Tolerant Design

6C.1: Design Methodology of Variable Latency Adders with Multistage Function Speculation

Yongpan Liu, Yinan Sun, Yihao Zhu, Huazhong Yang - Tsinghua University

6C.2: Accurate Statistical Soft Error Rate (SSER) Analysis

Yu-Shin Kuo, Huan-Kai Peng, Charles H.-P. Wen - National Chiao Tung University

6C.3: Measurement Circuits for Acquiring SET Pulse Width Distribution with Sub-F01-inverter-delay Resolution

Ryo Harada, Yukio Mitsuyama, Masanori Hashimoto, Takao Onoye - Osaka University

6C.4: Design of a Fault-Tolerant Coarse-Grained Reconfigurable Architecture: A Case Study

Syed M. A. H. Jafri, Stanislaw J. Pietrak, Olivier Sentieys, Sebastien Pillement - University of Rennes

6C.5: Comparative Analysis and Study of Metastability on High-Performance Flip-Flops

David Li, Pierce Chuan, Manoj Sachdev - University of Waterloo

6D: Quality System-Level Design

6D.1: Reliability Analysis of Analog Circuits by Lifetime Yield Prediction Using Worst-Case Distance Degradation Rate

Xin Pan and Helmut Graeb - Technische Universitaet Muenchen

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Dongkeun Oh, Nam Sung Kim, Yu Hen Hu - University of Wisconsin-Madison; Charlie Chung Ping Chen - National Taiwan University

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