PACT’08
Proceedings of the Seventeenth International Conference on Parallel Architectures and Compilation Techniques

Sponsored by:
ACM SIGARCH, IEEE-CS/TCCA, IFIP, & IEEE-CS/TCCP

Supported by:
Microsoft Research, Google, IBM, Intel, & AMD
Table of Contents

Organization.............................................................................................................. ix

Keynote

- GPU Evolution: Will Graphics Morph into Compute? ........................................... 1
  Norm Rubin (Advanced Micro Devices)

Session 1: Compilation

- Outer-Loop Vectorization — Revisited for Short SIMD Architectures .................. 2
  Dorit Nuzman, Ayal Zaks (IBM Haifa Research Laboratory)

- Redundancy Elimination Revisited ..................................................................... 12
  Keith Cooper, Jason Eckhardt, Ken Kennedy (Rice University)

- Exploiting Loop-Dependent Stream Reuse for Stream Processors ..................... 22
  Xuejun Yang, Ying Zhang (National University of Defence Technology, China),
  Jingling Xue (The University of New South Wales), Ian Rogers (The University of Manchester),
  Gen Li, Guibin Wang (National University of Defence Technology, China)

- Feature Selection and Policy Optimization for Distributed Instruction Placement Using
  Reinforcement Learning ....................................................................................... 32
  Katherine E. Coons, Behnam Robatmili, Matthew E. Taylor, Bertrand A. Maher, Doug Burger,
  Kathryn S. McKinley (University of Texas at Austin)

Session 2: CMP Architecture Design

- Core Cannibalization Architecture: Improving Lifetime Chip Performance for Multicore
  Processors in the Presence of Hard Faults .......................................................... 43
  Bogdan F. Romanescu, Daniel J. Sorin (Duke University)

- Pangaea: A Tightly-Coupled IA32 Heterogeneous Chip Multiprocessor ................ 52
  Henry Wong (University of British Columbia), Anne Bracy, Ethan Schuchman (Intel Corporation),
  Tor M. Aamodt (University of British Columbia), Jamison D. Collins, Perry H. Wang, Gautham Chinya,
  Ankur Khandelwal Groen, Hong Jiang, Hong Wang (Intel Corporation)

- Skewed Redundancy .......................................................................................... 62
  Gordon B. Bell (IBM Corporation), Mikko H. Lipasti (University of Wisconsin - Madison)

Session 3A: Analyzing Applications

- The PARSEC Benchmark Suite: Characterization and Architectural Implications .......... 72
  Christian Bienia (Princeton University), Sanjeev Kumar (Intel Corporation),
  Jaswinder Pal Singh, Kai Li (Princeton University)

- Visualizing Potential Parallelism in Sequential Programs .................................... 82
  Graham D. Price, John Giacomeni, Manish Vachharajani (University of Colorado)

- Characterizing and Modeling the Behavior of Context Switch Misses ................... 91
  Fang Liu, Fei Guo, Yan Solihin (North Carolina State University), Seongbeom Kim (VMWare Inc.),
  Abdulaziz Eker (The Scientific and Technical Research Council)

Session 3B: I/O Optimizations

- MCAMP: Communication Optimization on Massively Parallel Machines with
  Hierarchical Scratch-pad Memory ....................................................................... 102
  Hiroshige Hayashizaki, Yutaka Sugawara, Mary Inaba, Kei Hiraki (The University of Tokyo)

- Profiler and Compiler Assisted Adaptive I/O Prefetching for Shared Storage Caches .... 112
  Seung Woo Son, Sai Prashanth Muralidhara (Pennsylvania State University), Ozcan Ozturk (Bilkent University),
  Mahmut Kandemir (Pennsylvania State University), Ibrahim Kolcu (University of Manchester),
  Mustafa Karakoy (Imperial College)

- Runtime Optimization of Vector Operations on Large Scale SMP Clusters ............ 122
  Costin Iancu, Steven Hofmeyr (Lawrence Berkeley National Laboratory)
Keynote

- (How) Can Programmers Conquer the Multicore Menace? .................................................. 133
  Saman Amarasinghe (Massachusetts Institute of Technology)

Session 4: Multicore Memory Hierarchy Design (Part 1)

- Distributed Cooperative Caching ................................................................. 134
  Enric Herrero, Jose González, Ramon Canal (Universitat Politècnica de Catalunya)

- Scalable and Reliable Communication for Hardware Transactional Memory .................. 144
  Seth H. Pugsley, Manu Awasthi, Niti Madan, Naveen Muralimanohar,
  Rajeev Balasubramonian (University of Utah)

- Improving Support for Locality and Fine-Grain Sharing in Chip Multiprocessors .......... 155
  Hemayet Hossain, Sandhya Dwarkadas, Michael C. Huang (University of Rochester)

Session 5: Reconfigurable Architecture Optimization

- Edge-centric Modulo Scheduling for Coarse-Grained Reconfigurable Architectures ...... 166
  Hyunchul Park, Kevin Fan, Scott A. Mahlke (University of Michigan),
  Taewook Oh, Heesook Kim, Hong-seok Kim (Samsung Advanced Institute of Technology)

- Multi-Optimization Power Management for Chip Multiprocessors ............................. 177
  Ke Meng, Russ Joseph, Robert P. Dick (Northwestern University), Li Shang (University of Colorado)

- Multitasking Workload Scheduling on Flexible-Core Chip Multiprocessors ................. 187
  Divya P. Gulati (University of Texas at Austin), Changkyu Kim (Intel Corporation),
  Simha Sethumadhavan (Columbia University), Stephen W. Keckler, Doug Burger (University of Texas at Austin)

Session 6: Multicore Memory Hierarchy Design (Part 2)

- Leveraging On-Chip Networks for Data Cache Migration in Chip Multiprocessors ......... 197
  Noel Eisley, Li-Shiuan Peh (Princeton University), Li Shang (University of Colorado)

- Adaptive Insertion Policies for Managing Shared Caches ........................................ 208
  Aamer Jaleel, William Hasenplaug (Intel Corporation), Moimuddin Qureshi (IBM T.J. Watson Research Center),
  Julien Sebot (Intel Israel Design Center), Simon Steely Jr., Joel Emer (Intel Corporation)

- Analysis and Approximation of Optimal Co-Scheduling on Chip Multiprocessors .......... 220
  Yunlian Jiang, Xipeng Shen (College of William and Mary),
  Jie Chen (Thomas Jefferson National Accelerator Facility), Rahul Tripathi (University of South Florida)

Session 7: Multithreading Improvements

- An Adaptive Resource Partitioning Algorithm for SMT Processors ............................ 230
  Huaping Wang, Israel Koren, C. Mani Krishna (University of Massachusetts)

- Meeting Points: Using Thread Criticality to Adapt Multicore Hardware to Parallel Regions ......................................................... 240
  Qiong Cai, José González (Intel Barcelona Research Center), Ryan Rakvic (United States Naval Academy),
  Grigoris Magklis, Pedro Chaparro, Antonio González (Intel Barcelona Research Center)

Session 8: Middleware and Runtime Systems

- Prediction Models for Multi-dimensional Power-Performance Optimization on Many Cores ......................................................... 250
  Matthew Curtis-Maury, Ankur Shah, Filip Blagojevic, Dimitrios S. Nikolopoulos
  (Virginia Polytechnic Institute and State University),
  Bronis R. de Supinski, Martin Schulz (Lawrence Livermore National Laboratory)

- Mars: A MapReduce Framework on Graphics Processors ........................................... 260
  Bingsheng He, Wenbin Fang, Qiong Luo (Hong Kong University of Science and Technology),
  Naga K. Govindaraju (Microsoft Corporation), Tuyong Wang (Sina Corporation)

- Multi-mode Energy Management for Multi-tier Server Clusters ................................. 270
  Tibor Horvath, Kevin Skadron (University of Virginia)
Session 9: Programming the Memory Hierarchy

- **A Tuning Framework for Software-Managed Memory Hierarchies** .............................................. 280
  Manman Ren, Ji Young Park, Mike Houston, Alex Aiken, William J. Dally (Stanford University)

- **Hybrid Access-Specific Software Cache Techniques for the Cell BE Architecture** ........ 292
  Marc González (Universitat Politécnica de Catalunya and Barcelona Supercomputing Center),
  Nikola Vujic (Barcelona Supercomputing Center),
  Xavier Martorell, Eduard Ayguadé (Universitat Politécnica de Catalunya & Barcelona Supercomputing Center),
  Alexandre E. Eichenberger, Tong Chen, Zehra Sura, Tao Zhang, Kevin O’Brien,
  Kathryn O’Brien (IBM T.J. Watson Research Center)

- **COMIC: A Coherent Shared Memory Interface for Cell BE** ......................................................... 303
  Jaejin Lee, Sangmin Seo, Chihun Kim, Junghyun Kim, Posung Chun (Seoul National University),
  Zehra Sura (IBM T. J. Watson Research Center), Jungwon Kim, SangYong Han (Seoul National University)

**Author Index................................................................................................................................. 315**