An Update on IEEE 1149.6 - Successes and Issues .................................................. 536
Bill Eklow
IEEE 1500 Utilization in SOC Design and Test .......................................................... 543
Yervant Zorian, Avetik Yessayan
Layering Of The Stil Extensions .................................................................................. 553
Greg Maston, Tony Taylor
Analysis of Error-Masking and X-Masking Probabilities for Convolutional Compactors .................................................................................................................. 561
Masayuki Arai, Satoshi Fukumoto, Kazuhiko Iwasaki
XWRC: Externally-loaded Weighted Random Pattern Testing for Input Test Data Compression .............................................................................................................. 571
Seongmoon Wang, Kedarath J. Balakrishnan, Srinat T. Chakradhar
Test Data Compression for IP Embedded Cores Using Selective Encoding of Scan Slices .............................................................. 581
Zhanglei Wang, Krishnendu Chakrabarty
A Scalable Test Strategy For Network-On-Chip Routers .............................................. 591
Alexandre M. Amory, Eduardo Brito, Eríka Cota, Marcelo Lubaszewski, Fernando G. Moreira
On Concurrent Test of Wrapped Cores and Unwrapped Logic Blocks in SOCs ............ 600
Qiang Xu, Nicola Nicolici
Definition of a robust Modular SOC Test Architecture; Resurrection of the single TAM daisy-chain .......................................................... 610
Tom Waayers, Richard Morren, Roberto Grandi
Test Implications of Lead-Free Implementation in a High-Volume Manufacturing Environment .......... 620
Shu Peng, Sam Wang
Bead Probes in Practice ................................................................................................. 628
Kenneth P. Parker
Effect of Lead Free Solders on In-Circuit Test Process ................................................ 637
Rosa D. Reinosa
A Comprehensive Preemptive Test Solution for 1.5gb/S And 3gb/S Serial-Ata - Based On Awg and Undersampling Techniques .................................................. 644
Y. Cai, A. Bhattacharyya, J. Martone, A. Verma, W. Burchanowski
A Test Case for 3Gbps Serial Attached SCSI (SAS) ...................................................... 652
Y. Cai, L. Fang, R. Ruiemo, J. Liu, K. Gross, M. Kozma
Production-Oriented Interface Testing for PCI-Express by Enhanced Loop-Back Technique .................................................................................. 661
Mitchell Lin, Kwang-Ting (Tim) Cheng, Jimmy Hsu, MC Sun, Jason Chen, Shelton Lu
Towards Achieving Relentless Reliability Gains in a Server Marketplace of Teraflops, Laptops, Kilowatts, & "cost, Cost, COST".... (Making Peace between a Black Art and the Bottom Line) .......................................................... 671
Jody Van Horn
Test Connections - Tying Application to Process ........................................................... 679
John M. Carsulli Jr, Thomas J. Anderson
Logic Soft Errors A Major Barrier To Robust Platform Design ................................... 687
Subhasish Mitra, Ming Zhang, TM Mak, Norbert Seifert, Victor Zia, Kee Sup Kim
Built-In Constraint Resolution ....................................................................................... 697
Grady Giles, Joel Irby, Daniela Toneva, Kun-Han Tai
A Methodology For Testing One-Hot Transmission Gate Multiplexers ....................... 707
Teresa L. McLaurin, Frank Frederick, Rich Slobodnik
Hierarchical DFT with Enhancements for AC Scan, Test Scheduling and On-chip Compression - A Case Study .............................................................. 717
Richard Fisette, Jeffrey Remmers, Darin Lee
Enabling Yield Analysis with X-Compact ..................................................................... 726
Zoran Stanojevic, Rui Feng Guo, Subhasish Mitra, Srikanth Venkataraman
Use of MISRs for Compression and Diagnostics ............................................................ 735
Brion Keller, Thomas Bartenslein
Compressed Pattern Diagnosis For Scan Chain Failures .............................................. 744
Yu Huang, Wu-Ting Cheng, Janusz Rajski
Logic Proximity Bridges ............................................................................................... 752
Eric N Tran, Vamsi Krishna, Sutji Zarkariah, Sreejit Chakravarty
An Optimal Test Pattern Selection Method to Improve the Defect Coverage .......... 762
Yucin Tian, Michael R. Grimaila, Weiping Shi, M. Ray Mercer
Gate Exhaustive Testing ................................................................................................. 771
Kyoung Youn Cho, Subhasish Mitra, Edward J. McCluskey
JTAG-Based Vector And Chain Management For System Test ................................. 778
B. G. Van Treuren, B. E. Peterson, J. M. Miranda
Remote Boundary-Scan System Test Control for the ATCA Standard ....................... 788
David Bäckström, Gunnar Carlson, Erik Larsson
A Strategy For Board Level In-System Programmable Built-In Assisted Test And Built-In Self Test .............................................................. 798
Joshua Perry, Joseph Szanzak, Shoeb Shatik
JTAG (Internal JTAG): A Step Toward a DFT Standard ............................................. 808
Jeff Rearick, Bill Eklow, Ken Posse, Al Crouch, Ben Bennetts
Business Constraints Drive Test Decisions Planning, Partnerships and Success
Michael Campbell

Business Constraints Drive Test Decisions
Paul Domino

Panel: Business Constraints Drive Test Decisions
Jeff Schneider

Business Constraints Drive Test Decisions - not vice versa
Sanjiv Taneja

The ITC TEST COMPRESSION SHOOTOUT
Scott Davidson

Test Compression and Logic BIST at Your Fingertips
Shianling Wu, Laung-Terng (L.-T.) Wang, Jin Woo Cho, Zhigang Jiang, Boryau Sheu

Encounter Test OPMISR + On-Chip Compression
Brion Keller

XMAX: A Practical and Efficient Compression Architecture
Kee Sup Kim

Test Compression - Real Issues and Matching Solutions
Janusz Rajski

Methods for Improving Test Compression
Nur A. Touba

Have we overcome the Challenges associated with SoC and Multi-Core Testing?
Sankaran Menon

Panel discussion for "Have we overcome the Challenges associated with SoC and Multi-Core testing?"
Nathan Chelstrom

Have We Overcome The Challenges Associated With SoC and Multi-Core Testing?
Rajesh Raina

Position Statement: "Have we overcome the challenges associated with SoC and multi-core testing?"
Tim Wood

Today's SOC Test Challenges
Yervant Zorian

Panel Synopsis: Reducing High-Speed/RF Test Cost: Guaranteed by Design or Guaranteed to Fail?
Hosam Haggag, Abhijit Chatterjee

Darwin, Thy Name is System
Craig Force

Reducing High-Speed/RF Test Cost-Guaranteed by Design or Guaranteed to Fail?
Mustapha Slamani

Guaranteed by Design or Guaranteed to Fail or Guaranteed by Test? or ... Neither?
Mani Soma

Correct by Construction is Guaranteed to Fail
Stephen Sunter

Achieving Higher Yield Through Diagnosis
Nagesh Tamarapalli

Needs Fabless Yield Ramp Foundry Partnership To Be Most Successful
Bruce Cory

Achieving Higher Yield Through Diagnosis- The Asic Perspective
Chris Schueermann

Achieving Higher Yield through Diagnosis?
Srikant Venkataraman

Partnering with Customer to Achieve High Yield
James Wang

The Final D-Frontier: Should DFT be Outsourced?
Luis Basto

Outsourcing DFT: The Right Mix
Carl Holzwarth

Off-Shore Outsource DFT vs. Build Off-Shore Branch Offices
Yu Huang

The case for outsourcing DFT
Jeffrey L. Roehr

Outsourcing DFT: It can be done but it isn't easy
LeRoy Winemberg

Test The Test Experts: Do We Know What We Are Doing?
Rohit Kapur