PROCEEDINGS
The 2004 IEEE Asia-Pacific Conference on
Circuits and Systems

SoC Design for Ubiquitous Information Technology

December 6-9, 2004
Tayih Landis Hotel, Tainan, Taiwan

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Technical Sessions

1A: System LSI Design
01:20pm – 03:00pm, December 7
Room: Athens

1A.1: A Stable Multi-Level Partitioning Algorithm Using Adaptive Connectivity Threshold
Jin-Kuk Kim, Jong-Wha Chong, Hanyang University, Korea; Satoshi Goto, Waseda University, Japan

1A.2: Video Coding Algorithm Based on Adaptive Tree for Low Electricity Consumption
Seiichiro Hiratsuka, Fukuoka Industrial Science and Technology Foundation, Japan; Satoshi Goto, Takaaki Baba, Takeshi Ikenaga, Waseda University, Japan

1A.3: On The Effectiveness of Dynamically Allocating Resources Across Program Execution Phases for Media Workloads
Subhasis Banerjee, G. Surendra, S. K.Nandy, Indian Institute of Science, India

1A.4: A Reconfigurable Adaptive FEC System for Reliable Wireless Communications
Kazunori Shimizu, Takeshi Ikenaga, Masao Yanagisawa, Satoshi Goto, Tatsuo Ohtsuki, Waseda University, Japan; Nozomu Togawa, the University of Kitakyushu & Waseda University, Japan

1A.5: CMOS System LSI for Processing IEEE 802.11b WLAN PHY Signals Through Digital, Analog Baseband, and RF

1B: VLSI Arithmetic
01:20pm – 03:00pm, December 7
Room: Berlin

1B.1: Booth Memoryless Modular Multiplier With Signed-Digit Number Representation
Shuangching Chen, Shugang Wei, Kensuke Shimizu, Gunma University, Japan

1B.2: High-Speed VLSI Design for Montgomery Inverse over GF(2m)
Jun-Hong Chen, Ming-Der Shieh, National Cheng Kung University, Taiwan; Chien-Ming Wu, Chip Implementation Center, Taiwan

1B.3: Power-Aware Design of an 8-Bit Pipelining Asynchronous ANT-Based CLA Using Data Transition Detection
Chua-Chin Wang, Ching-Li Lee, and Pai-Li Liu, National Sun Yat-Sen University, Taiwan
1B.4: An Alternative Scheme of Redundant Binary Multiplier
*Chip-Hong Chang, Yajuan He, Jiangmin Gu,* Nanyang Technological University, Singapore

1B.5: Design of Reconfigurable Array Multipliers and Multiplier-Accumulators
*Chin-Long Wey, Jin-Fu Li,* National Central University, Taiwan

1C: Mixed Technology Systems
01:20pm – 03:00pm, December 7
Room: London

1C.1: A Speech Codec with a Class AB Switch-Current Sigma-Delta Modulator and an Area-efficient Decimator/Interpolator
*Shuenn-Yuh Lee, Chih-Jen Cheng,* National Chung-Cheng University, Taiwan

1C.2: A Low Voltage High Unity-Gain Bandwidth CMOS OP-AMP
*Chih-Min Yu, Zhi-Ming Lin, Jun-Da Chen,* National Changhua University of Education, Taiwan

1C.3: A Multi-Mode LDO-Based Li-Ion Battery Charger in 0.35μm CMOS Technology
*Chia-Chun Tsai, Chin-Yen Lin, Yuh-Shyan Hwang, Wen-Ta Lee, Trong-Yen Lee,* National Taipei University of Technology, Taiwan

1C.4: Design of a High-Transimpedance CMOS Receiver for 600 Mb/s Optical Communications
*S. Guessab, P. Benabes, R. Kielbasa,* SUPÉLEC, France

1C.5: A Design of Programmable AC Voltage and Current Generators for Testing Energy Meters
*Sarawoot Methawee, Ekachai Leelarasmee,* Chulalongkom University, Thailand

1D: Modeling and Simulation
01:20pm – 03:00pm, December 7
Room: New York

1D.1: 3D Electro-Thermal Modeling of GGNMOS ESD Protection Structure
*Haolu Xie, Rouying Zhan, Albert Wang,* Illinois Institute of Technology, USA; R. Gafiteanu, Synopsys, USA

1D.2: A Petri Net Based Timing Model for Hardware/Software Co-Design of Digital Systems
*N. Marranghello,* Sao Paolo State University, Brazil; W. L. A. de Oliveira, F. Damiani, University of Campinas, Brazil

1D.3: Accurate RT-Level Power Estimation Using Up-Down Encoding
*Ming-Yi Sum, Shi-Yu Huang, Chia-Chien Weng, Kai-Shuang Chang,* National Tsing-Hua University, Taiwan
1D.4: A Distributed State Variables Approach to the Transmission Lines
Ekachai Leelarasme, Praphun Naenna, Chulalongkorn University, Thailand

1D.5: A Multithreaded HDL Simulator for Deep Submicron SOC Designs
Terence Chan, TJ Systems, USA

1E: Signal Coding and Processing
01:20pm – 03:00pm, December 7
Room: Paris

1E.1: Lossless Image Compression Via Multi-Scanning and Adaptive Linear Prediction
Tang Haijiang, Kamata Sei-ichiro, Waseda University, Japan; Tsuneyoshi Kazuyuki, Kitakyushu Foundation for the Advancement of Industry, Science and Technology, Japan; Kobayashi Masa-aki, Panasonic Electronics Ltd, Japan

1E.2: Hadamard Transform Based Fast Codeword Search Algorithm for High-Dimensional VQ Encoding
Shu-Chuan Chu, Kuang-Chih Huang, Cheng Shiu University, Taiwan; Zhe-Ming Lu, Harbin Institute of Technology, China; Jeng-Shyang Pan, Harbin Institute of Technology, China & National Kaohsiung University of Applied Sciences, Taiwan

1E.3: A Fast Fractal Image Coding Using Pyramid Structure of Image Blocks
Chou-Chen Wang, Liang-Chi Lin, I-Shou University, Taiwan; Jung-Yang Kao, Industrial Technology Research Institute, Taiwan

1E.4: Representation of 1/f Signal Via Multiwavelet Bases
Xiaohong Yan, Guizhong Liu, Feng Liu, Xi’an Jiaotong University, China

1E.5: A Novel Approach for Image Morphing
Ngo Quoc Tao, Nguyen Duc Long, Vietnamese Academic Science and Technology, Vietnam

2A: RFIC (I)
03:20pm – 05:00pm, December 7
Room: Athens

2A.1: A 3.5 GHz 2 W MMIC Power Amplifier Using AlGaAs/InGaAs/GaAs PHEMTs
Chen-Kuo Chu, Hou-Kuei Huang, Hong-Zhi Liu, Ray-Jay Chiu, Che-Hung Lin, Chih-Cheng Wang, Yeong-Her Wang, National Cheng-Kung University, Taiwan; Chuan-Chien Hsu, Wang Wu, Chang-Luen Wu, Chian-Sern Chang, Transcom, Inc. Taiwan

2A.2: High Linearity Power Amplifier for PHS Base Station Using a 50 mm AlGaAs/InGaAs/GaAs PHEMT

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2A.3: A 1 V 2.4 GHz CMOS Power Amplifier with Integrated Diode Linearizer
Kun-Yi Lin, Ro-Min Weng, Chih-Lung Hsiao, Hung-Che Wei, National Dong Hwa University, Taiwan

2A.4: Chip Set Design for 10 Gb/s Optical Transceiver
Li-Ren Huang, Chia-Ming Tsai, Cheng-Yu Chien, Chien-Fu Chang, and Day-Uei Lee, Industrial Technology Research Institute, Taiwan

2A.5: Design of a 12.8-GB/S Inp HBT Limiting Amplifier with Cross-Point Control for Driving a Distributed Modulator Driver
David H. Chiang, Texas A&M University-Kingsville, USA; Bert K. Oyama, Northrop Grumman, USA

2B: VLSI Architecture
03:20pm – 05:00pm, December 7
Room: Berlin

2B.1: A Novel Programmable Digital Signal Processor for Multimedia Applications
Li-Chun Lin, Tay-Jyi Lin, Chen-Chia Lee, Chie-Min Chao, Shin-Kai Chen, Chia-Hsien Liu, Pi-Chen Hsiao, Chih-Wei Liu, Chein-Wei Jen, National Chiao-Tung University, Taiwan

2B.2: An Universal VLSI Architecture for Bit-Parallel Computation in GF(2m)
Chien-Ching Lin, Fuh-Ke Chang, Hsie-Chia Chang, Chen-Yi Lee, National Chiao-Tung University, Taiwan

2B.3: Efficient DSP Architecture for Viterbi Decoding with Small Trace Back Latency
Jeong Hoo Lee, Jong Ha Moon, Myung H. Sunwoo, Ajou University, Korea; Weon Heum Park, Samsung Electronics, Korea

2B.4: A Novel SoC Architecture Embedded Bit Serial FPGA
Yiwen Wang, Dongju Li, Tsuyosi Isshiki, Hiroaki Kunieda, Tokyo Institute of Technology, Japan

2B.5: CDMA-Based Network-on-Chip Architecture
Daewook Kim, Manho Kim, Gerald E. Sobelman, University of Minnesota, USA

2C: Video Codec & Rate Control
03:20pm – 05:00pm, December 7
Room: London

2C.1: A Bit-Allocation Model Using on-Line Rate-Distortion Optimization in MPEG-4 Rate Control
Zhongwei Zhang, Guizhong Liu, Yongli Li, Min Zhang, Xi'an Jiaotong University, China

2C.2: A Survey of Error Resilient Coding Schemes for Image and Video Transmission Based on Data Embedding
Li-Wei Kang, Jin-Jang Leou, National Chung Cheng University, Taiwan

2C.3: Implementation of Half-Pel Motion Estimation IP Core for MPEG-4 ASP@L5 Texture Coding
He Wei-feng, Gao Zhi-qiang, Mao Zhi-gang, Zhang Yan, Harbin Institute of Technology, China

2C.4: Reconfigurable Low Power MPEG-4 Texture Decoder IP Design
Chien-Chang Lin, Hsiu-Cheng Chang, Jiun-In Guo, Kuan-Hung Chen, National Chung Cheng University, Taiwan

2C.5: Rate Control by Partial Differential Equation Modeling
Zhongwei Zhang, Guizhong Liu, Hongliang Li, Xi’an Jiaotong University, China

2D: Design Automation and Testing
03:20pm – 05:00pm, December 7
Room: New York

2D.1: Experimental Evaluation of High-Level Energy Optimization Based on Thread Partitioning
Jumpei Uchida, Yuichiro Miyaoka, Masao Yanagisawa, Tatsuo Ohtsuki, Waseda University, Japan; Nozomu Togawa, the University of Kitakyushu & Waseda University, Japan

2D.2: A Reusable Methodology for Non-Slicing Floorplanning
Jer-Ming Hsu, National Center of High-Performance Computing, Taiwan; Yao-Wen Chang, National Taiwan University, Taiwan

2D.3: Zero-Skew Clock Algorithms for High Performance System on a Chip
Yen-Tai Lai, Yung-Chuan Jiang, Cheng-Hsiung Tsai, National Cheng Kung University, Taiwan

2D.4: An on-Chip Concurrent High Frequency Analog and Digital Sinusoidal Signal Generator
Hsin-Wen Ting, Bin-Da Liu, Soon-Jyh Chang, National Cheng Kung University, Taiwan

2D.5: Efficient Testing and Design-For-Testability Schemes for Multimedia Cores: a Case Study on DCT Circuits
Ming-Der Shieh, Sheng-Chih Shen, You-Chung Lin, Kuen-Jong Lee, National Cheng Kung University, Taiwan

2E: Speech Coding and Enhancement
03:20 – 05:00pm, December 7
Room: Paris

2E.1: An Efficient Speech Enhancement Method using Kalman Filter and Spectral Subtraction
Chi-Chou Kao, National Pingtung Institute of Commerce, Taiwan; Yen-Tai Lai, National Cheng Kung University, Taiwan

2E.2: Improving G.728’s Hybrid Window and Excitation Gain
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Gang Zhang, Keming Xie, Xueying Zhang, Liying Huangfu, Taiyuan University of Technology, China

2E.3: Wavelet Statistical Model of Speech for Feature Extraction and Denoising
Shao Yu, Tong Y. C., Wang Chao, Nanyang Technological University, Singapore

2E.4: A Computationally Efficient Noise Estimation Algorithm for Speech Enhancement
V. G. Reju, Tong Yit Chow, Nanyang Technological University, Singapore

2E.5: Fine Granularity Scalability for MP-CELP Based Speech Coding with HPDR Technique
Supattarachai Chompun, Kasetsart University, Thailand

P1: POSTER SESSION
01:20pm – 03:20pm, December 7
Room: Victory

Communication Systems

P1.1: Improving the Clipped OFDM Performance by Using Conic Function
Linjun Wu, Shihua Zhu, Xingle Feng, Xi'an Jiaotong University, China

P1.2: Design and Simulation of a MIMO OFDM Baseband Transceiver for High Throughput Wireless LAN
Chi-Yeh Yu, Zih-Yin Ding, Tzi-Dar Chiueh, National Taiwan University, Taiwan

P1.3: A Novel Encoding/Decoding Technique of Space-Time Block Coded Transceiver for IEEE 802.11a Wireless Local Area Network
Gwo-Ruey Lee, Cheng-Lun Yang, Jyh-Horng Wen, National Chung Cheng University, Taiwan

P1.4: An Improved MIMO Detector for High Data Rates Wireless Communications
Zhan Guo, Peter Nilsson, Lund University, Sweden

P1.5 Low Power Correlator of DSP Core for Communication System
Ya-Lan Tsao, Jun-Xian Teng, Maw-Ching Lin, National Central University, Taiwan; Shyh-Jye Jou, National Chiao Tung University, Taiwan

P1.6: Digital RDS Demodulation in FM Subcarrier Systems
Jui-Yuan Lin, Kuang-Hao Lin, Southern Taiwan University of Technology, Taiwan; Shuen-Yuh Lee, National Chung-Cheng University, Taiwan

P1.7: Laser/Modulator Driver with High Modulation Output Operating up to 14-Gb/s Using 0.35μm SiGe BiCMOS Process
Day-Uei Li, Chia-Ming Tsai, Li-Ren Huang, Industrial Technology Research Institute, Taiwan
P1.8: Application of Dual Projected Pseudo Quasi Newton Algorithm in Multicommodity Network Flow Problems
Ch'i-Hsin Lin, Kao Yuan Institute of Technology, Taiwan; Shin-Yeu Lin, National Chiao Tung University, Taiwan

P1.9: OC-48 Generic Frame Mapping Device for WAN Accessing
Po-Chun Chiang, Chih-Feng Cheng, Industrial Technology Research Institute, Taiwan

P1.10: A Realization of Diversity Waveform Sets for Delay-Doppler Imaging
Shu-Ming Tseng, Guan-Fu Huang, Yuan Ching Tzeng, and Wen-Chi Tseng, National Taipei University of Technology, Taiwan; Der-Feng Tseng, National Taiwan University of Science and Technology, Taiwan

Analog Circuits

P1.11: Design of Low-Power Switched-Capacitor Filter with Switched-OPAMP Technique
Shuenn-Yuh Lee, Shyh-Chyang Lee, National Chung-Cheng University, Taiwan

P1.12: A Low Power and High-Speed Current Latched Comparator for Weak Current Operations
Ro-Min Weng, Chia-Wei Chiang, National Dong Hwa University, Taiwan

P1.13: Design Techniques for Low-Voltage Micropower CMOS Switched-Capacitor Delta-Sigma Modulator
Tsung-Sum Lee, Wen-Bin Lin, Dung-Lin Lee, National Yunlin University of Science and Technology, Taiwan

P1.14: A Sizing Methodology For A Low-Noise Comparator
Kuo-Hsin Lai, Shi-Yu Huang, Pei-Chia Chiang, National Tsing-Hua University, Taiwan

P1.15: A Rail-To-Rail Constant Gain CMOS OP-Amp
Yung-Chih Liang, Meng-Lieh Sheu, Wei Hung Hsu, National Chi-Nan University, Taiwan

P1.16: A Novel Ultra-High Speed Signal Capture Based on a Single FPGA Chip
Guo-Ruey Tsai, Min-Chuan Lin, Kun-Shan University of Technology, Taiwan; Jen-Wei Hsieh, Yun-Chung Lin, Kaoshiung University of Applied Science, Taiwan

RFIC

P1.17: A CMOS Infrared Optical Preamplifier with a Variable-Gain Transimpedance Amplifier
Roger Yubitzuan Chen, Chih-Yuan Hung, Tsung-Shueng Hung, National Yunlin University of Science and Technology, Taiwan

P1.18: Design and Analysis of A CMOS Even Harmonic Mixer with Current Reuse Circuits
Ming-Feng Huang, Shuenn-Yuh Lee, Chung J. Kuo, National Chung Cheng
PI.19: A Novel Low Noise Design Method for CMOS L-Degeneration Cascoded LNA
Sung-Huang Lee, Ying-Zong Juang, Chin-Fong Chiu, National Chip Implementation Center, Taiwan; Hwann-Kaeo Chiou, National Central University, Taiwan

PI.20: A 0.6 V CMOS Low Noise Amplifier for 2.4GHz Application
Chih-Lung Hsiao, Ro-Min Weng, Kun-Yi Lin, National Dong Hwa University, Taiwan

PI.21: An Evaluation of SiGe/Si HBT High Efficiency Power Amplifiers for Wide Dynamic Power Control Range Application
Cheng-Chieh Lin, Ping-Chun Yeh, Hwann-Kaeo Chiou, National Central University, Taiwan

PI.22: A Fully Integrated 5.2GHz CMOS Inductively Degenerated Low Noise Amplifier
Ruey-Lue Wang, National Kaohsiung Institute of Marine Technology, Taiwan; Huang-Wei Chen, Chih-Ho Tu, Kan Shan University of Technology, Taiwan; Jian-Shiuan Liou, National Cheng Kung University, Taiwan

PI.23: A 1.5 V 2.4 GHz CMOS Mixer with High Linearity
Hung-Che Wei, Ro-Min Weng, Chih-Lung Hsiao, Kun-Yi Lin, National Dong Hwa University, Taiwan

PI.24: A 2 V CMOS Low Noise Amplifier with Tunable Image Filtering
Ro-Min Weng, Pei-Shan Lin, National Dong Hwa University, Taiwan

PI.25: Analysis of LO Leakage Due to LO Mismatch in CMOS Gilbert Mixer for Direct Conversion Application
J. J. Liu, M. A. Do, J. G. Ma, K. S. Yeo, Nanyang Technological University, Singapore

PI.26: A Low Voltage 900MHz Voltage Controlled Ring Oscillator with Wide Tuning Range
Yun-Hsueh Chuang, Sheng-Lyang Jang, Jian-Feng Lee, Shao-Hua Lee, National Taiwan University of Science and Technology, Taiwan

PI.27: A 1.8-V Monolithic SiGe HBT Power Amplifier with a Novel Proposed Linearizing Bias Circuit
Ping-Chun Yeh, Kuei-Cheng Lin, C. Y. Lee, Hwann-Kaeo Chiou, National Central University, Taiwan

PI.28: Analysis of LO Leakage in CMOS Gilbert Mixer by Cadence SpectreRF for Direct Conversion Application
M. A. Do, J. J. Liu, K. S. Yeo, J. G. Ma, Nanyang Technological University, Singapore

PI.29: An 1.25 Gbit/s −29 dBm Burst-Mode Optical Receiver Realized with
0.35 um SiGe BiCMOS Process Using a PIN Photodiode
Chun-Chi Chen, Chia-Ming Tsai, Li-Ren Huang, Industrial Technology Research Institute, Taiwan

DSP and Parallel Processing
P1.30: Hardware Design in Statement Level Parallel Processing
Kosei Shimoo, Akira Yamawaki, Masahiko Iwane, Kyushu Institute of Technology, Japan

3A: RF IC (II)
01:20pm – 03:00pm, December 8
Room: Athens

3A.1: CMOS RF LNA with High ESD Immunity
Siu-Kei Tang, Cheong-Fat Chan and Chiu-Sing Choy, Kong-Pang Pun, the Chinese University of Hong Kong, Hong Kong

3A.2: A 1 V 1.1 GHz CMOS Integrated Receiver Front-end
Wang-Chi Cheng, Cheong-Fat Chan, Kong-Pang Pun, Chiu-Sing Choy, the Chinese University of Hong Kong, Hong Kong

3A.3: Analysis and Improvement on Propagation Efficiency of High-Speed Asymmetric Differential Transmission System
Ding-Bing Lin, Ji-Liang Pan, National Taipei University of Technology, Taiwan

3A.4: Performance Trade-Offs in Designing a Dual-Band CMOS IEEE 802.11a/b Frontend
Kittichai Phansathitwong, Henrik Sjoland, Lund University, Sweden

3A.5: Symbol-Spaced Delay Circuit Design with Half-Rate Clock Timing for Multi-Taps FIR Filter as Pre-Emphasis
Miao Li, Tad Kwasniewski, Peter Noel, Carleton University, Canada

3B: VLSI — Digital Circuits
01:20pm – 03:00pm, December 8
Room: Berlin

3B.1: An Ultra Low-Power Output Feedback Flip-Flop
Myint Wai Phyu, Wang Ling Goh, Kiat Seng Yeo, Nanyang Technological University, Singapore

3B.2: 0.75-V Sub-threshold CMOS Logic Using Dynamic Substrate Bias
Yu-Cherng Hung, Bin-Da Liu, National Cheng Kung University, Taiwan

3B.3: Leakage Current Reduction in CMOS Logic Circuits
Heng-Yao Lin, Chi-Sheng Lin, Lih-Yih Chiou, Bin-Da Liu, National Cheng Kung University, Taiwan

3B.4: Two Efficient Area Reduction Methods for Implementations of the Rijndael Advanced Encryption Standard
Shen-Fu Hsiao, Ming-Chih Chen, National Sun-Yat Sen University, Taiwan
3B.5: A Chaos-Based Fully Digital 120 MHz Pseudo Random Number Generator
Hsing-Tsung Yang, Jing-Reng Huang, Tsin-Yuan Chang, National Tsing Hua University, Taiwan

3C: DSP and Computer Arithmetic
01:20pm – 03:00pm, December 8
Room: London

3C.1: A Module Generator for Parameterized DSP Core
Ya-Lan Tsao, Yu-Chun Lin, Wei-Hao Chen, Bo-Shiang Huang, National Central University, Taiwan; Shyh-Jye Jou, National Chiao Tung University, Taiwan

3C.2: Digital Signal Processor Architectures and Programming
Sen M. Kuo, Northern Illinois University, USA; Woon S. Gan, Nanyang Technological University, Singapore

3C.3: Real-Time 3D Computation Using LUT-Based DSP Systems
Hakim Khali, Mehdi Riyadh, Abdulaziz Araar, Ajman University of Science & Technology Network, UAE

3C.4: A Low-Cost and Application-Driven Digital Signal Processor for Speech/Audio Processing
Jen-Feng Chung, Chin-Teng Lin, National Chiao-Tung University, Taiwan

3C.5: A New RNS to Mixed-Radix Number Converter Using Modulo \((2^P - 1)\) Signed-Digit Architecture
Shugang Wei, Kensuke Shimizu, Gunma University, Japan

3D: Communication System (I)
01:20pm – 03:00pm, December 8
Room: New York

3D.1: A Variable-Length DHT-Based FFT/IFFT Processor for VDSL/ADSL Systems
Tsung-Chieh Pao, Ching-Chi Chang, Chorng-Kuang Wang, National Taiwan University, Taiwan

3D.2: Spatial Correlation of a Circular Array Antenna and BER Performance Investigation
Kenta Ishizawa, Jie Zhou, Shigenobu Sasaki, Shogo Muramatsu, Hisakazu Kikuchi, Niigata University, Japan

3D.3: Baseband Transceiver Design for the DVB-Terrestrial Standard
Yi-Ju Chen, Yi-Ching Lei, Tzi-Dar Chiueh, National Taiwan University, Taiwan

3D.4: Design of Partially Adaptive STBC CDMA Receiver Using Conjugate Gradient Algorithm
Gau-Joe Lin, Ta-Sung Lee, National Chiao Tung University, Taiwan; Tsui-Tsai Lin, National United University, Taiwan
3D.5: Design of Common Structures for CDMA Systems
Sung Dae Kim, Myung H. Sunwoo, Seong K. Oh, Ajou University, Korea; Sug H. Jeong, DAEWOO Electronics Corp., Korea

3E: Digital Filter Design and Algorithms
01:20pm – 03:00pm, December 8
Room: Paris

3E.1: Efficient Weighted $L_p$ Algorithm for the Design of Low-Pass FIR Filters with Some Closed-Form Derivations
Yue-Dar Jou, Tain-Shou Nien, Military Academy, Taiwan

3E.2: Design and Application of Variable Fractional Order Differentiator
Chien-Cheng Tseng, National Kaohsiung First University of Science and Technology, Taiwan

3E.3: A Design Method of Multi-Channel Cyclic Filter Banks with Less Multiplications by Genetic Algorithm
F. Itami, Saitama Institute of Technology, Japan; E. Watanabe, Shibaura Institute of Technology, Japan; A. Nishihara, Tokyo Institute of Technology, Japan

3E.4: Dedicated Structure for Tunable Multiband FIR Filters with Linear Phase and Maximally Flat Magnitude
Saed Samadi, M. Omair Ahmad, M.N.S. Swamy, Concordia University, Canada; Akinori Nishihara, Tokyo Institute of Technology, Japan

3E.5: Design of 2-D FIR Digital Filters with Symmetric Properties by Genetic Algorithm Approach
Shian-Tang Tzeng, Kaoyuan Institute of Technology, Taiwan

4A: RF IC (III)
03:20pm – 05:00pm, December 8
Room: Athens

4A.1: A Low Jitter Phase-Lock Loop Based on a New Adaptive Bandwidth Controller
Chel Hur, YoungShig Choi, HyekHwan Choi, TaeHa Kwon, Pukyong National University, Korea

4A.2: A New LC-Tank Voltage Controlled Oscillator
Shao-Hua Li, Sheng-Liang Jang, Yun-Sheh Chuang, Chien-Feng Li, National Taiwan University of Science and Technology, Taiwan

4A.3: Design of a Dual-Band 5/2.4 GHz CMOS VCO for 802.11 a/b/g WLAN Transceivers
Ali Fard, Tord Johnson, Denny Aberg, Malardalen University, Sweden

4A.4: A 1-V 2.4-GHz CMOS Frequency Synthesizer with Current-Match Charge Pump
Chung-Yu Wu, Chih-Yuan Hsieh, Wei-Ming Chen, National Chiao-Tung University, xxx
Taiwan

4A.5: Handover Considerations in VCO Design for Multistandard Wireless Receiver
V. Vibhute, R. Veljanovski, J. Singh, A. Zayegh, A. Stojcevski, Victoria University, Australia

4B: VLSI — Digital Signal Processing
03:20pm – 05:00pm, December 8
Room: Berlin

4B.1: Design of a System-on-Chip for ECG Signal Processing
Meng-chou Chang, Zong-xin Lin, Che-wei Chang, Hsiao-lung Chan, Wu-shiung Feng, Chang Gung University, Taiwan

4B.2: Complexity-Aware Design of DA-Based FIR Filters
Chih-Chao Chen, Tay-Jyi Lin, Chih-Wei Liu, Chein-Wei Jen, National Chiao Tung University, Taiwan

4B.3: A New Dynamic Scaling FFT Processor
Yu-Wei Lin, Chen-Yi Lee, National Chiao Tung University, Taiwan

4B.4: A Maskable Memory Architecture for Rank-Order Filter
Meng-Chun Lin, Lan-Rong Dung, National Chiao Tung University, Taiwan

4B.5: Low-Error Carry-Free Fixed-Width Multipliers and Their Application to DCT/IDCT
Tso-Bing Juang, National Sun Yat-sen University & Ta Jen Institute of Technology, Taiwan; Shen-Fu Hsiao, Shiann-Rong Kuang, Ming-Yu Tsai, National Sun Yat-sen University, Taiwan

4C: Networking
03:20pm – 05:00pm, December 8
Room: London

4C.1: A Novel BIB-Based Parallel Download Scheme
Chih-Hung Chao, Jung-Shian Li, National Cheng Kung University, Taiwan

4C.2: Network Planning and Capacity Management Considering Adaptive Sectorization in Survivable FDMA/CDMA Systems
Kuo-Chung Chu, National Taiwan University & Jin-Wen Institute of Technology, Taiwan; Frank Yeong-Sung Lin, National Taiwan University, Taiwan

4C.3: Improving RPR Fairness Convergence
Chuan-Gang Liu, Jung-Shian Li, National Cheng Kung University, Taiwan

4C.4: Optimizing One-to-One Data Communication on Double-Loop Networks
Hsun-Wen Chang, Ching-Wen Yu, Tatung University, Taiwan

4C.5: System Optimization of Contents Delivery Network with Information-Zooming Function

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4D: Communication Systems (II)
03:20pm – 05:00pm, December 8
Room: New York

4D.1: Adaptive Receivers with PN Code Tracking for DS-CDMA Communications
Fang-Biau Ueng, Jun-Da Chen, Shang-Chun Tsai, National Chung-Hsing University, Taiwan

4D.2: Simultaneous Bidirectional PAM-6 Wired Link with Adaptive Pre-Emphasis and Trellis Coding
Ming-ta Hsieh, Gerald E. Sobelman, University of Minnesota, USA

4D.3: Performance Bounds for Block Transmission System
Farid Ghani, University Sains Malaysia, Malaysia

4D.4: A New Technique for Digital Compensation in IQ Modulator
A. G. K. C. Lim, V. Sreeram, G. Wang, University of Western Australia, Australia

4D.5: Determination of Bandwidth and Free Spectral Range for the Silicon Based Ring Resonators and Racetrack Microcavity Resonators
S. Khuntaweetep, S. Somkuarnpanit, K. Sae-Tang, King Mongkut’s Institute of Technology-Ladkrabang, Thailand

4E: Adaptive Algorithms and Filters
03:20pm – 05:00pm, December 8
Room: Paris

4E.1: A New Variable Step Size Method for the LMS Adaptive Filter
Junibakti Sanubari, Satya Wacana University, Indonesia

4E.2: Adaptive Two-Stage LQ Reliable Control of Uncertain Discrete-Time Systems
Chien-Shu Hsieh, Ta Hwa Institute of Technology, Taiwan

4E.3: Adaptive Lowpass Filters
Kentaro Yamaguchi, Akinori Nishihara, Tokyo Institute of Technology, Tokyo, Japan; Eiji Watanabe, Shibaura Institute of Technology, Japan

4E.4: Sound Minimisation for Local Active Control
Wen-Kung Tseng, Nankai Institute of Technology, Taiwan

4E.5: Optimal Design of Stable Recursive Digital Filter Using Unconstrained Optimization Methods
Osemekhian I. Omoifo, Takao Hinamoto, Hiroshima University, Japan

P2: POSTER SESSION
01:20pm – 03:20pm, December 8
Room: Victory
Physical Design Automation

P2.1: Removing Operation of Empty Rooms on Sequence-Pair
Chikaaki Kodama, Kunihiro Fujiiyoshi, Tokyo University of Agriculture. & Technology, Japan

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P2.24: Low Complexity Variable-Size Block-Matching Motion Estimation for Adaptive Motion Compensation Block Size in H.264
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P2.25: VLSI Architecture Design for Variable-Size Block Motion Estimation in MPEG-4 AVC/H.264
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5A: Analog Circuits (I)
08:30am – 10:10am, December 9
Room: Athens

5A.1: A 10-bit 350-MSample/s Nyquist CMOS D/A Converter
Jeng-Dau Chang, Hsin-Hung Ou, Bin-Da Liu, National Cheng Kung University, Taiwan

5A.2: Design of High-Resolution Pipelined Analog-to-Digital Converters Using Multiple-Phase Capacitor-Splitting Feedback Interchange Technique
Chih-Haur Huang, Soon-Jyh Chang, Kuen-Jong Lee, National Cheng Kung University, Taiwan

5A.3: Filter Design with Voltage Conveyors
Vit Novotny, Vaclav Zeman, Brno University of Technology, Czech Republic

5A.4: A Portable and Wireless Data Transmission Potentiostat
Chun-Yueh Huang, Huan-Yu Lin, Yu-Chien Wang, Kun Shan University of Technology, Taiwan; Wei-Yin Liao, Tse-Chuan Chou, National Cheng Kung University, Taiwan

5A.5: Automated Phase Compensation for Multi-Stage Amplifiers
Naoyuki Unno, Naoto Kusakawa, Shigetaka Takagi, Nobuo Fujii, Tokyo Institute of Technology, Japan

5B: Power Conversion and Power Electronics
08:30am – 10:10am, December 9
Room: Berlin

5B.1: Application of Maximum-Efficiency Tracking Control for Backlight Module Based on Phase-Locked Loop Technique
Chang-Hua Lin, Ying Lu, St. John’s & St. Mary’s Institute of Technology, Taiwan; Yu-Kang Lo, Kai-Jun Pai, National Taiwan University of Science & Technology, Taiwan

5B.2: High Performance PMLSM Drives Using TMS320F2812