2003
PROCEEDINGS
TWENTIETH INTERNATIONAL
VLSI MULTILEVEL
INTERCONNECTION
CONFERENCE
(VMIC)

A SPECIALTY CONFERENCE OF
TWENTIETH INTERNATIONAL VLSI MULTILEVEL INTERCONNECTION CONFERENCE September 23 - 25, 2003 ADVANCE PROGRAM

Tuesday, September 23, 2003 OPENING SESSION — 9 A.M.
Welcoming Remarks by the General Chairman Dr. Thomas E. Wade University of South Florida

SESSION I — 9:15 A.M.
KEYNOTE ADDRESS
MICRO/NANOELECTRONICS - PAST, PRESENT AND FUTURE
Dr. Yoshio Nishi
Director, Stanford Nanofabrication Facility
STANFORD UNIVERSITY
Stanford, California

Coffee Break 9:45 - 10:00 A.M.

SESSION II - 10:00 A.M. - 12:00 P.M.
VLSI MULTILEVEL INTERCONNECTION DIELECTRIC SYSTEMS
Chairman: Dr. Willi Volksen
IBM ALMADEN RES. CENTER
San Jose, California


2.E “Process Integration of NANOGGLASS E Porous Ultra Low-k Material (k = 2.2) With Copper Metallization” by X.T. Chen, Y.W. Chen, B. R. Murthy, S. Balakumar, C. Y. Li, C.K. Chang, M. Mukherjee-Roy, Y. J. Su; INST. OF MICROELECTRONICS; SINGAPORE; and A. Naman; HONEYWELL; Sunnyvale, CA. 50

POSTER PAPERS

2.F “Perovskite High-k Dielectrics for Frequency Agile Applications” by C.J. Wang, C.Y. Hung, D.G. Chou L.M. Chen; UNION CHEMICAL; Taiwan, R.O.C. 59

2.G “Evaluation of Single Wafer Wet Cleans With Organic Spin-On Dielectric Materials (Porous SILK)” by L. Archer; SEZ AMERICA; Phoenix, AZ.; and M. Simmonds, K. Itchhaporia; DOW CHEMICAL; Midland, MI.

2.H “Mechanical and Electrical Strength Improvement for Low Dielectric Constant Materials” by Y.L. Huang, S.H. Lin, Z.C. Wu, T.J. Chou, W. Chang, S.M. Jang, M.S. Liang; T.S.M.C.; Taiwan, R.O.C. 67

2.I “Integration of Ultra Low-k Aurora With Copper Damascene Metallization” by C.F. Tsang, S. Balakumar, C.Y. Li, V. Bliznetsovy, A. Krishnamoorthy, Y.J. Su; INST. OF MICROELECTRONICS; SINGAPORE; and N. Matsuki; ASM JAPAN; Tokyo, JAPAN.

SESSION III - 1:30 - 3:30 P.M.
VLSI MULTILEVEL INTERCONNECTION VMI CMP PROCESSES
Chairman: Dr. Katia Devriendt
I.M.E.C.
Leuven, Belgium

CMP CONDUCTOR PROCESSES

3.A “Robust Copper Abrasive-Free Polishing For 90 Nanometer Node Process” by Y. Yamada and N. Konishi; HITACHI LTD; Tokyo, JAPAN. 85 (Invited Paper)

3.B “Optimizing Tungsten CMP In The Age of Copper” by R. Donis, J. Kalpathy-Cramer, J. Pallinetti and D. Vijay; LSI LOGIC; Gresham, OR. 94

3.C “Copper CMP Planarity and With-In-Die Rs Improvements on 90 nm Copper / Low-k Interconnects” by W. Hong, C.W. Chiou, Y.H. Chen, S.M. Jang and M.S. Liang; T.S.M.C.; Taiwan, R.O.C. 102
3.D “Copper CMP Process With a Two-Chemistry Slurry on a Linear Belt Polisher” by R. Small, B. Scott and P. Chelle; DUPONT EKC TECH; Hayward, CA.; and Y. Fang, R. Charatan, C. Sainio and P. Cheng; LAM RESEARCH; Fremont, CA. 108

3.E “Process and Yield Improvement by Changing Consumables in Tungsten CMP” by R. Lin and J. Tung; PROMOS TECH; Taiwan, R.O.C.; and L. Nguyen, T. West, S. Kirtley and G. Wu; THOMAS WEST; Sunnyvale, CA. 115

3.F “Copper CMP Process Development for Copper / Ultra Low-k Materials” by S. Balakumar, T. Selvaraj, B. Lin, Y.W. Chen, M. Mukherjee-Roy, R. Kumar; INST. OF MICRoeLECTRONICS; SINGAPORE; and J. Chee; CABOT MICRO; SINGAPORE. 119

3.G “CMP Process for Copper / Low-k Interlayer Multilevel Interconnections” by S. Balakumar; INST. OF MICRoeLECTRONICS; SINGAPORE; and T. Hara; HOSEI UNIV.; Tokyo, JAPAN. 125

3.H “Ability of Preventing Delamination for Low-k Film With Air Float Concept CMP Head in Copper CMP” by A. Ueno, T. Yokoyama, A. Yamane and A. Isobe; ACCRETECH; Tokyo, JAPAN. 135

SESSION IV - 3:40 - 5:00 P.M.

VLSI MULTILEVEL INTERCONNECTION PROCESS CHARACTERIZATION

Chairman: Dr. Maximilian Biberger
SUPERCritical SYSTEMS, INC.
Gilbert, Arizona

3.I “A Study on CMP Scratches” by G. Fu; IOWA STATE UNIV.; Ames, IA. 145

3.J “A Study Toward Edge Exclusion 1 mm: Substrate Shape and Polishing Profile Correlation” by T. Fukui, K. Tanaka, M. Numoto, A. Yamane and A. Isobe; ACCRETECH; Tokyo, JAPAN. 149


4.D “Copper / Low-k Cleaning Approach for Advanced Interconnect Device Applications” by C. Waldfried, Q. Han, O. Escorcia and I. Berry; AXCELIS TECH; Rockville, MD.; and E. Andideh; INTEL CORP; Hillsboro, OR. 180

4.E “Golden Parameter Ratio Application in the WEB Recipe Development” by J. Zhang and G. Magsamen; ST MICROELECTRONICS; Carrollton, TX; and A. Sidhwa; ST MICROELECTRONICS; Phoenix, AZ. 189

4.F “Patterning of Copper Using Microcontact Printing of SAMs” by N.H. Kim, E.G. Chang; CHUNG-ANG UNIV.; Seoul, KOREA; J.H. Lim; GROWELL TELECOM; Seoul, KOREA; Y.J. Seo; DAEBUL UNIV.; Chonnam, KOREA; and S.Y. Kim; ANAM SEMICONDUCTOR; Kyunggi-do, KOREA. 193


4.H “Evaluation of a Zirconium Oxide Coated Belljar and Quartz Insulator Used For a Soft Sputter Etch Process” by A. Sidhwa, M. Goulding, T. Gandy and C. Spinner; ST MICROELECTRONICS; Phoenix, AZ; and D. Laube, I. Davis; BOC EDWARDS; Phoenix, AZ. 201

4.I “Impact Reliability of Solder Joints on Bond-Pad” by M. Date and K.N. Tu; UCLA; Los Angeles, CA.; T. Shoji, M. Fujiyoshi and K. Sato; HITACHI METALS; Yasugi, JAPAN. 205


4.K “Development of SiCr Thin Film Resistor in Si and SiGe RF-BiCMOS Technology” by H. Sun, K.M. Lau and P. McDonald; PHILIPS SEMICONDUCTOR; Hopewell Junction, N.Y. 213

4.L “Elimination of Aluminum Cube, Abnormal Aluminum Grains and Wafer Breakage by Modifying the High Temperature Clamp Ring Used in Aluminum PVD Deposition Chambers” by A. Sidhwa, M. Goulding, T. Gandy and C. Spinner; ST MICROELECTRONICS; Phoenix, AZ. 217

4.M “Impact of Substrate Thickness on CMOS LC-VCO” by Y.Z. Xiong and A.B. Ajikuttira; INST. OF MICROELECTRONICS; SINGAPORE. 221
SESSION V - 9:00 - 10:20 A.M.
VLSI MULTILEVEL INTERCONNECTION
3D INTEGRATED CIRCUIT REALIZATION

Chairman: Dr. Richard Allen
NAT'L INST of STD & TECH (NIST)
Gaithesburg, Maryland

5.A “Wafer Level 3D Hyper-Integration” by J.Q. Lu, Y. Kwon, J.J. McMahon, A. Jindal, T.S. Cale; R.J. Gutmann; RENSSELAER POLYTECH. INST; Troy, N.Y.; B. Altemus, D. Cheng, E. Eisenbraun; UNIV of ALBANY; Albany, N.Y.
(Invited Paper)


(Invited Paper)

(Invited Session)

SESSION VI - 10:35 A.M. - 12:15 P.M.
VLSI MULTILEVEL INTERCONNECTION CURRENT ART & SCIENCE OF CMP

Chairman: Dr. David Stein
SANDIA NAT'L LABS
Albuquerque, New Mexico

6.A “More Than Density: Pattern Dependencies in the Copper Era” by T. Smith, T.G. Tugbawa, R. Moore, D. White, B. Lee, K.H. Chen and V. Mehrotra; PRAESAGUS; San Jose, CA.
(Invited Paper)

6.B “Removing Contaminants From Wafer Edge, Back Side and Hydrophobic Front Side in Post-CMP Cleaning System” by M. Ravkin, J. deLarios, J. Farber; LAM RESEARCH; Fremont, CA.
(Invited Paper)

6.C “Chemical and Electrochemical Characterization of Peroxide-Induced Passivation of Copper in Aqueous Glycine Solutions” by F. Doyle and L. Wang; UNIV. Of CALIFORNIA; Berkeley, CA.
(Invited Paper)

6.D “Modeling Chemical-Mechanical Polishing” E. Paul; STOCKTON COLLEGE; Pomona, N.J.
(Invited Paper)

6.E “Copper CMP: Issues, Current and Future” by M. Oliver; RODEL; Newark, DE.
(Invited Paper)

SESSION VII
VLSI MULTILEVEL INTERCONNECTION CONDUCTOR SYSTEMS

— POSTER PAPERS —

7.A “A Novel Fabrication of Copper Interconnection by Displacing the Pre-Patterned Ti Film for ULSI” by C.H. Yang, W.L. Yang, D.G. Liu, T.J. Yang and G.S. Chen; FENG CHIA UNIV.; Taiwan, R.O.C.

7.B “Studies of Various Effects on the Tungsten Film Used for High Aspect Ratio Plug Fill” by J. H. Zhang, G. Magsamen; ST MICRO-ELECTRONICS; Carrollton, TX; and A. Sidhwa; ST MICROELECTRONICS; Phoenix, AZ.

7.C “Resistivity of 75 nm Node Copper Interconnection Layer - Reduction of Resistivity in Electroplated Copper Line” by T. Hara and Y. Shimura; HOSEI UNIV; Tokyo, JAPAN.


7.E “Aging Effects of PEG and SPS on Filling Capability of Copper Electrochemical Deposition” by T.C. Li, C. Chen; CHIAO TUNG UNIV.; J.M. Shieh, B.T. Dai; N.N.D.L.; S.C. Chang, Y.L. Wang; T.S.M.C.; and J. Ting; MERCK-KANTO CHEMICAL; Taiwan, R.O.C.

7.F “The Influence of Nitrogen on Tungsten Film Stack Deposited at 425°C and 475°C Temperature for Interconnect Applications” by A. Sidhwa, M. Gonsalves, X. Breurec, M. Goulding and T. Gandy; ST MICRO-ELECTRONICS; Phoenix, AZ.

SESSION VIII - 1:15 - 2:15 P.M.
VLSI MULTILEVEL INTERCONNECTION POSTER PAPER / EXHIBITION
DEDICATED VIEWING TIME
SESSION IX - 2:15 - 5:15 P.M.
VLSI MULTILEVEL INTERCONNECTION
CMP PROCESSES

Chairman:
Dr. Anantha Sethuraman
FEI COMPANY
Sunnyvale, California

**CMP MODEL & SIMULATION**

9.A “Model Based Wafer-to-Wafer Control for Copper CMP” by F. Ko, J.S. Lin, P.H. Chen, S. Wu, H. Lo, M.S. Zhou and M.S. Liang; T.S.M.C.; Taiwan, R.O.C.; and J. Zou, T. Mullins, J. Moyne and K. Edwards; BROOKS AUTOMATION; Andover, MI. 323

9.B “The Oxide CMP Auto Feed Back System Optimization by Multivariables Regression Model” by Y. Huang, S. Wang, A. Su and J.C.S. Chu; PROMOS TECH; Taiwan, R.O.C. 331

9.C “A Comprehensive Material Removal Model for Chemical Mechanical Planarization” by W. Che, Y. Guo, A. Chandra and A. Bastawros; IOWA STATE UNIV.; Ames, IA. 340

**CMP CONSUMABLES**

9.D “Development of Slurries for Selective and Non-Selective Polishing Schemes Using SILK Integrated Wafers” by D. Merricks, S. Mao and B. Her; FERRO CORP; Penn Yan, N.Y.; and K. Itchhaporia, M. Simmonds; DOW CHEMICAL; Midland, MI. 353


9.F “Chemically Enhanced Copper Polishing With Abrasive-Free “Micelle Slurry”- Part II” by K. Okita, H. Ishimura, S. Funakoshi and H. Takahashi; ASAHI KASEI; Kanagawa, JAPAN; and T.K. Doy; SAITAMA UNIV.; Saitama, JAPAN. 363

9.G “Effects of Oxidizer Additive on the Performance of Copper Chemical Mechanical Polishing Using Tungsten Slurry” by W.S. Lee; G.W. Choi, CHOSUN UNIV.; Gwang-Ju, SOUTH KOREA; Y.J. Seo; DAEBUL UNIV; Chonnam, KOREA. 373


9.I “Studies on Copper Damascene Barrier Slurries: Semiconductor Dissolution in Chemical Mechanical Planarization Process” by S. Mao, D. Merricks and B. Her; FERRO CORP; Penn Yan, N.Y. 382

9.J “Oxide CMP Characteristics of Mixed Abrasive Slurry by Adding of Annealed Alumina Powder” by Y.J. Seo, C.J. Park; DAEBUL UNIV; Chonnam, KOREA; W. Lee; CHOSUN UNIV; Gwang, KOREA. 390

9.K “CMP Pad Conditioners With Diamond Grid” by J. Sung; KINK; Taiwan, R.O.C. 394

9.L “Aging Effects of Silica Slurry and Oxide CMP Characteristics” by W.S. Lee, P.J. Ko; CHOSUN UNIV.; Gwang, KOREA; Y.J. Seo; DAEBUL UNIV; Chonnam, KOREA. 394


**CMP PROCESS**

--- POSTER PAPERS ---

9.N “Dynamic Pot-Life and Handling Evaluation of Rodel RLS3126 Reactive Liquid Copper Clearing Chemistry” by B. Johl, A. Manzonic; RODEL; Phoenix, AZ. 413

**CMP DIELECTRICS**


--- POSTER PAPERS ---

9.P “CMP Characteristics of Ferroelectric Film Fabricated by Sol-Gel Method for FRAM Applications” by Y.J. Seo, S.W. Park; DAEBUL UNIV.; Chonnam, KOREA; W.S. Lee;CHOSUN UNIV;Gwang, KOREA. 427

**POST-CMP CLEANING**

--- POSTER PAPERS ---

9.Q “Evaluation of Benzotriazole Removal Capabilities of Several Copper Post-CMP Cleaners” by E. Walker, S. Naghshineh and D. Peters; ATMI; Bethlehem, PA. 433
SESSION X - 8:15 - 10:15 P.M.
VLSI MULTILEVEL INTERCONNECTION
MODELING & EXTRACTION OF PARASITICS IN I.C.'s

Chairman: Dr. Kausik Chatterjee
CALIFORNIA STATE UNIVERSITY
Fresno, California


10.B “Modeling of Distributed Parasitic Effects in FETS and New 4-Port Equivalent Circuit for Small Gate-Width FET Building Blocks” by S. Lee and R. Roblin; OHIO STATE UNIV.; Cleveland, OH. 445

(Invited Paper)


10.D “The Evolution of Metal Grain Size Distributions” by T.S. Cale and M.O. Bloomfield; RENSSELAER POLYTECH. INST.; Troy, N.Y. 455

(Invited Paper)

10.E “Accurate Nanometer Copper Interconnect Inductance Modeling Using Giga-Hertz Wafer Measurements” by K.J Chang; TSING HUA UNIV.; Taiwan, R.O.C.; and L. F. Chang; SEQUENCE DESIGN; Santa Clara, CA. 464

10.F “Modeling of Two Coupled Transmission Lines in Even and Odd Mode” by J. Diao, Y. Tretiakov, Y. LeCoz, and J.F. McDonald; RENSSELAER POLYTECH. INST.; Troy, N.Y. 471

--- POSTER PAPERS ---

10.G “The Modeling of Temperature Distribution on a Vertical LPCVD Furnace for Film Deposition in Advanced Deep Trench DRAM” by C. Wang; PROMOS TECH; Taiwan, R.O.C. 477

(Invited Session)
SESSION XI - 10:30 A.M. - 12:15 P.M.
VLSI MULTILEVEL INTERCONNECTION
CMP TRIBO-METROLOGY

Chairman: Dr. Norman Gitis
CENTER for TRIBOLOGY
Campbell, California

11.A “Thickness Measurement Method of Dielectric Film on LSI Patterns Using Waveform Analysis of Multi-Spectral Reflectance” by T. Hirose, M. Nomoto; HITACHI; Yokohama, JAPAN; and T. Arai; RENESAS TECH; Tokyo, JAPAN. 483

11.B “CMP Process and Consumable Evaluation With PadProbe” by J. Fang, K.M. Davis; IBM; East Fishkill, N.Y.; N.V. Gitis and M. Vinogradov; CTR. For TRIBOLOGY; Campbell, CA. 491

11.C “Next Generation Materials for CMP Retaining Rings” by R. Moussa; GREENE, TWEED & CO; Kulpsville, PA. 497

11.D “Incoming Inspection and Failure Analysis of CMP Consumables at the Semiconductor Fab” by N.V. Gitis, M. Vinogradov; CTR. For TRIBOLOGY; Campbell, CA. 505

2003 VMIC LUNCHEON
Thursday, September 25; 12:30 - 2:00 P.M.
Luncheon Presentation
(1:30 - 2:00 PM)
“THREE DIMENSIONAL INTEGRATION:
THE NEXT FRONTIER FOR SEMICONDUCTORS”
Dr. Siva Sivaram
MATRIX SEMICONDUCTOR
San Jose, California

(Invited Session)
SESSION XII - 2:00 - 4:00 P.M.
VLSI MULTILEVEL INTERCONNECTION
CMP PARTICLE & SLURRY INNOVATIONS

Chairman: Dr. Yuzhuo Li
CLARKSON UNIVERSITY
Potsdam, New York

12.A “Effect of Surface Charges on Silicon Dioxide and Nitride Planarization Using Alumina/Ceria Mixed Abrasive Slurries” by S. Hegde and S.V. Babu; CLARKSON UNIV; Potsdam, N.Y. 519

(Invited Paper)
12.B “A Novel Slurry Designed for High Copper/Barrier Selectivity and Low Friction Copper CMP” by N. Wang; TACH TECHNOLOGY; Martinez, CA; and J. Keleher, K. Rushing, A. Vitale, M. Hayward and Y. Li; CLARKSON UNIV; Potsdam, NY


12.D “Chemical Analysis of Slurry Components After Silicon Oxide CMP” by W. America; IBM; East Fishkill, N.Y.; J. Keleher, and K. Rushing; CLARKSON UNIVERSITY; Potsdam, N.Y.

12.E “Particle Innovations for Copper CMP” by S. Hellring; PPG; Monroeville, PA.

SESSION VIII
VLSI MULTILEVEL INTERCONNECTION
RELIABILITY ISSUES

—— POSTER PAPERS ——

13.A “A Study of Failure Mode in High Aspect Ratio Contacts” by L.H. Li, K.Y. Tseng, T.J. Hong and W.C. Lien; MACRONIX; Taiwan, R.O.C.

13.B “High Via-1 Chain Resistance Resulting From Excessive Soft Sputter Etch and Thick Titanium Layer Deposition at a High Temperature” by S. Toh, K. Liu, G. Magsamen, P. Sagarwala; ST MICROELECTRONICS; Carrollton, TX; and A. Sidhwa; ST MICROELECTRONICS; Phoenix, AZ.


13.D “The Impact of Thermal Budget Causing High Via Resistance Failure for 0.18 micron Memory Products” by C. Consalvo, A. Privitera; D. Mello; ST MICROELECTRONICS; Canania, ITALY; A. Sidhwa; ST MICROELECTRONICS; Phoenix, AZ; and L. Marzaioli; APPLIED MATERIALS; Catania, ITALY.


13.F “Understanding of the High Via Resistance Problem Due to Poor Quality of Isolation Ceramic Part” by R. Petri, L. LePrevost, L. Carrier, M.P. Nabot-Henaff; ST MICROELECTRONICS; Roussel, FRANCE; A. Sidhwa; ST MICROELECTRONICS; Phoenix, AZ.