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Thursday, November 6, 2003

10:00 REGISTRATION

Welcome and Plenary Session
Chairpersons: A. Morino (Selete), T. Arikado (Selete)
10:30-10:40 Opening Remark
A. Morino (Selete)
10:40-11:05 Keynote Speech
T. Nishitani (NEC)

High-k 1 Session
Chairperson: A. Toriumi (Univ. of Tokyo)
11:05-11:40 HiK1_1 Invited: Hf-based High-K Dielectrics
J. C. Lee
The University of Texas at Austin, USA
11:40-12:15 HiK1_2 Invited: Implementation of High-k gate dielectrics - a status update
S. De. Gendt¹, J. Chen², R. Carter, E. Cartier², M. Caymax¹, M. Claes¹, T. Conard¹, A. Delabie¹, W. Deweerd¹, V. Kaushik², A. Kerber², S. Kubicek¹, J. W. Maes³, M. Niwa⁴, L. Pantisano¹, R. Puurunen¹, L. Ragnarsson¹, T. Schram¹, Y. Shimamoto⁵, W. Tsai², E. Rohr¹, S. Van. Elshocht¹, T. Witters¹, E. Young², C. Zhao¹ and M. Heyns¹
¹IMEC, ²ISMT, ³ASM, ⁴Matsushita, ⁵Hitachi/Renesas, ⁶KULeuven, Belgium
12:15-13:30 Lunch

Poster Session
13:30-15:00

HK-1 Degradation of Dielectric Characteristics of Underlying Ultrathin SiO₂ films by Al Adsorption in High Vacuum
M. Tanabe¹, M. Goto¹, A. Uedono¹ and K. Yamabe¹,²
¹Institute of Applied Physics, ²Tsukuba Research Center for Interdisciplinary Materials Science, University of Tsukuba, Japan

HK-2 The Influence of Silicon Nitride Cap on NBTI and Fermi Pinning in HfO₂ Gate Stacks
T. Sasaki, F. Ootsuka, T. Hoshi, T. Kawahara, T. Maeda, M. Yasuhira and T. Arikado
Semiconductor Leading Edge Technologies, Inc. (Selete), Japan
HK-3 Vapor-Liquid Hybrid Deposition (VALID) of Hafnium Silicate Films Using Hf(O'C,H₉)₄ and Si(OC₂H₅)₄ Precursors
Y. Xuan and T. Yasuda
MIRAI, Advanced Semiconductor Research Center (ASRC), National Institute of Advanced Industrial Science and Technology (AIST), Japan

HK-4 Electrical characteristics of rare-earth oxides stacked-layer structures
S. Ohmi¹, I. Ueda², Y. Kobayashi², K. Tsutsui¹ and H. Iwai²
¹ Interdisciplinary Graduate School of Science & Engineering, ² Frontier Collaborative Research Center, Tokyo Institute of Technology, Japan

HK-5 Effects of Hf sources, Oxidizing Agents, and NH₃ Radicals on Properties of HfAlOₓ Films Prepared by Atomic Layer Deposition
T. Kawahara, K. Torii, R. Mitsuhashi, A. Mutoh, A. Horiuchi, H. Ito and H. Kitajima
Semiconductor Leading Edge Technologies, Inc. (Selete), Japan

HK-6 Charge State Dependent Point Defect in High-κ Dielectric HfO₂
K. Shiraishi¹, M. Saito² and T. Ohno²
¹ Institute of Physics, University of Tsukuba, ² National Research Institute of Material Science, Japan

HK-7 Solution-based fabrication of high-κ gate dielectrics
Y. Aoki and T. Kunitake
Topochemical Design Lab., Frontier Research System, RIKEN, Japan

HK-8 Improvement in the uniformity and the thermal stability of Hf-silicate gate dielectric by plasma-nitridation
Semiconductor Leading Edge Technologies, Inc. (Selete), Japan

HK-9 Gate Dielectrics on Strained-Ge layers on Si₁₋ₓGeₓ/Si Virtual Substrates
S. Bhattacharya¹, J. McCarthy³, B. M. Armstrong¹, H. S. Gamble¹, G. K. Dalapati², S. Das², C. K. Maiti², T. Perova³ and A. Moore³
¹ School of Electrical & Electronic Engineering, The Queen's University of Belfast, UK, ² Department of Electronics & ECE, Indian Institute of Technology, Kharagpur, India, ³ Department of Electrical & Electronic Engineering, Trinity College, University of Dublin, Ireland

TO-1 Method of increasing gate nitridation and its impact on CMOS devices
V. P. Gopinath, V. Hornback⁺, Y. Le⁺, A. Kamath, L. Duong⁺, J. Lin⁺, M. R. Mirabedini and W. C. Yeh
Advanced Device Development, ⁺ Process Module Development, ⁺ Device Characterization, LSI Logic Corporation, USA
TO-2 Nitrogen-related Enhanced Reliability Degradation in nMOSFETs with 1.6 nm Gate Dielectric
1 Institute of Electronics, National Chiao-Tung University,
2 National Nano Device Laboratories, Taiwan

TO-3 Ultra-Thin SiN Gate Dielectric Fabricated by N\textsubscript{2} Plasma Direct Nitridation
M. Inoue, J. Tsuchimoto, M. Mizutani, J. Yugami, Y. Ohno and M. Yoneda
Process Development Dept., Wafer Process Engineering Development Div., LSI Manufacturing Technology Unit, Renesas Technology Corp., Japan

FE-1 Effects of Interactions between HfO\textsubscript{2} and Poly-Si on MOSCAP and MOSFET Electrical Behavior
1 International SEMATECH, USA
IMEC, Belgium

FE-2 Improved performance of FETs with HfAlO\textsubscript{x} gate dielectrics using optimized poly-SiGe gate electrodes
A. Muto, H. Ohji, T. Kawahara, T. Maeda, K. Torii and H. Kitajima
Semiconductor Leading Edge Technologies, Inc. (Selete), Japan

RE-1 Self-organized Si suboxide (SiO\textsubscript{x}, x<2) interfacial layers - optimization of performance and reliability in advanced devices
G. Lucovsky and J. C. Phillips
1 North Carolina State University, Department of Physics,
2 Rutgers University, USA

RE-2 Impacts of Hole Trapping on the NBTI Degradation and Recovery in PMOS Devices
1 National Nano Device Laboratories,
2 Institute of Electronics, National Chiao-Tung University, Taiwan

MO-1 Resonant tunneling in stacked dielectrics: a novel approach for obtaining the electron tunneling mass-condution band offset energy products for gate dielectrics
C. L. Hinkle, C. Fulton, R. J. Nemanich and G. Lucovsky
North Carolina State University, Department of Physics, USA

MO-2 Proposal of quantum well gate insulating (QWGI) structures for band offset engineering from first-principles calculation
T. Shimizu and T. Yamaguchi
Advanced LSI Technology, Corporate R&D Center, Toshiba Corp., Japan
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**High-k 2 Session**

Chairperson: T. Yasuda (AIST)

15:00-15:35 **HiK2_1** Invited: Atomic layer deposition chemistry, mechanisms and related physical properties of high permittivity dielectric oxides

K. Kukli
University of Helsinki, Department of Chemistry, Finland
University of Tartu, Institute of Experimental Physics and Technology, Estonia

15:35-15:55 **HiK2_2** Separate and independent control of interfacial band alignments and constants in complex rare-earth/transition metal (Re/Tm) oxides

G. Lucovsky¹, Y. Zhang¹, J. L. Whitten², D. G. Scholm³ and J. L. Freecur⁴
¹ Dept. of Physics, ² Dept. of Chemistry, North Carolina State University,
³ Dept. of Materials Science and Engineering, Pennsylvania State University,
⁴ Dept. of Electrical and Computer Engineering, Oregon Graduate Institute, USA

15:55-16:15 **HiK2_3** Study of defects in MOS structures using HfAIOₓ gate dielectric by means of positron annihilation

A. Uedono¹, R. Mitsuhashi², A. Horiuchi², K. Torii², K. Yamabe¹, K. Yamada³, R. Suzuki⁴, T. Ohdaira⁴ and T. Mikado⁴
¹ Institute of Applied Physics, University of Tsukuba,
² Semiconductor Leading Edge Technologies, Inc. (Selete),
³ Nano Technology Research Laboratory, Waseda University,
⁴ National Institute of Advanced Industrial Science and Technology, Japan
16:30-17:05 FET1  
Invited: Gate Dielectric Scaling for High-Performance CMOS: from SiO$_2$ to High-k  
R. Chau, S. Datta, M. Doczy, J. Kavalieros and M. Metz  
*Intel Corporation, USA*

17:05-17:40 FET2  
Invited: Electrical and Physical Properties of Poly-Si Gated HfSiON Gate Dielectrics  
H. Niimi  
*Texas Instruments, USA*

17:40-18:00 FET3  
Invited: HfSiON Gate Dielectric for CMOS Applications  
$^1$SoC R & D Center, $^2$Process & Manufacturing Engineering Center, Toshiba Corporation Semiconductor Company, $^3$Corporate R & D Center, Toshiba Corporation, Japan
Friday, November 7, 2003

9:00 REGISTRATION

Thin SiON Session

Chairpersons: S. Kimura (Hitachi), H. Watanabe (NEC)

9:30-10:05 SiON1 Invited: Extending the Life of N/O Stack Gate Dielectric with Gate Electrode Engineering
Q. Xiang, Z. Krivokapic, W. Maszara and M.-R. Lin
Technology Development Group, Advanced Micro Devices, Inc., USA

10:05-10:40 SiON2 Invited: Advanced Oxynitride Gate Dielectrics for CMOS Applications
J. Yugami, S. Tsujikawa, T. Tsuchiya, S. Saito, Y. Shimamoto, K. Torii,
T. Mine and T. Onai
LSI Manufacturing Technology Unit, Wafer Process Engineering Development Div., Renesas Technology Corp.,
Central Research Laboratory, Hitachi Ltd., Japan

10:40-11:00 SiON3 Drastically Improved NBTI Lifetime By Periodic Plasma Nitridation for 90nm Mobile Applications at Low Voltage Operation
T. Kawae1, Y. Minemura1, S. Fukuda2, T. Hirano2, Y. Suzuki2, M. Saito2,
S. Kadomura2 and S. Samukawa1
Institute of Fluid Science, Tohoku University,
Semiconductor Network Company, SONY Corporation, Japan

11:00-11:20 SiON4 Improvement in thermal stability of the interfacial layer for poly-Si/HfAlO, gate stacks
R. Mitsuhashi1, A. Horiuchi1, A. Uedono2 and K. Torii1
Semiconductor Leading Edge Technologies, Inc. (Selete),
Institute of Applied Physics, University of Tsukuba, Japan

11:20-11:30 Break

Modeling 1 Session: Interfacial Property

Chairperson: C. Kaneta (Fujitsu Labs.)

11:30-12:05 M1_1 Invited: Atomic Scale Study of High-k Gate Dielectrics
K. J. Cho
Stanford University, USA

12:05-13:20 Lunch

Modeling 2 Session: Carrier Mobility

Chairperson: S. Takagi (AIST, Univ. of Tokyo)

13:20-13:55 M2_1 Invited: Reduced Electron Mobility in High-k MOSFETs Due to Insulator Optical Phonons: Density, Temperature and Material Dependence
M. V. Fischetti
IBM, USA
13:55-14:15  M2_2  Comparative Study of Carrier Mobility and Threshold Voltage between N- and P-MOSFETs in TaN Gate CMOS with EOT=1.5-2nm HfAlO_x
H. Ota¹, H. Hisamatsu², N. Yasuda², W. Mizubayashi¹, M. Ohno², K. Iwamoto², K. Tominaga³, M. Kadomishi³, N. Yamagishi³, K. Akiyama³, K. Yamamoto³, T. Nabatame², T. Horikawa¹ and A. Toriumi¹,³
¹ MIRAI, Advanced Semiconductor Research Center (ASRC), ² MIRAI, Association of Super-Advanced Electronics Technologies (ASET), ³ Department of Materials Science, The University of Tokyo, Japan

14:15-14:35  M2_3  Dependence of Electron Mobility by Remote Coulomb Scattering on Dielectric Constant Distribution in Stacked Gate Dielectrics
M. Ono, T. Ishihara and A. Nishiyama
Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation, Japan

14:35-14:45  Break

High-k 3 Session 169

Chairpersons: K. Shiraishi (Univ. of Tsukuba), Y. Akasaka (Selete)

14:45-15:20  HiK3_1  Invited: EOT Scaling and Device Issues for High-k Gate Dielectrics
M. I. Gardner¹, S. Gopalan, J. Gutt, J. Peterson¹, H.-J. Li² and H. R. Huff
International SEMATECH, ¹ Advanced Micro Devices, ² Intel, ³ Infineon, USA

15:20-15:40  HiK3_2  In-situ HfSiON/SiO₂ gate dielectric fabrication using hot wall batch system
Semiconductor Leading Edge Technologies, Inc. (Selete), Japan

15:40-16:00  HiK3_3  Effects of Nitrogen Incorporation into HfAlO_x Films on Gate Leakage Current - From XPS Study of Hf Bonding States
T. Nishimura¹, K. Iwamoto², K. Tominaga², T. Yasuda¹, W. Mizubayashi¹, S. Fujii², T. Nabatame² and A. Toriumi¹,³
¹ MIRAI, Advanced Semiconductor Research Center (ASRC), ² National Institute of Advanced Industrial Science and Technology (AIST), ³ MIRAI, Association of Super-Advanced Electronics Technologies (ASET), AIST

16:00-16:20  HiK3_4  Further EOT Scaling of Ge/HfO₂ over Si/HfO₂ Systems
K. Kita, M. Sasagawa, K. Tomida, M. Tohyama, K. Kyuno and A. Toriumi
Department of Materials Science, School of Engineering, The University of Tokyo, Japan

16:20-16:30  Break
Panel Discussion 16:30-18:30

Development Strategy of Gate Dielectrics: Ultra-thin Oxynitride versus High-k Materials
Organizers: H. Iwai (Tokyo Inst. of Technol.), M. Hiratani (Hitachi, T. I. Tec), M. Takayanagi (Toshiba), H. Kitajima (Selete)
Moderator: H. Iwai (Tokyo Inst. of Technol.)
Potential Panelists: H.-K. Kang (Samsung)
T. Horikawa (AIST(MIRAI))
K. Torii (Selete)
Y. Tsunashima (Toshiba)
J. Yugami (Renesas)
S. De Gendt (IMEC)
H. Niimi (Texas Instruments)
M. V. Fischetti (IBM)
R. Chau (Intel)

Closing Session 18:30-18:35

Closing Remark
F. Ootsuka (Selete)