2000
PROCEEDINGS
FIFTH INTERNATIONAL
CHEMICAL-MECHANICAL
PLANARIZATION
FOR
ULSI MULTILEVEL
INTERCONNECTION
CONFERENCE
(CMP-MIC)

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FIFTH INTERNATIONAL
C.M.P. PLANARIZATION
FOR ULSI MULTILEVEL INTERCONNECTION
CONFERENCE

Thursday, March 2, 2000

OPENING SESSION - 8:00 A.M.
Welcoming Remarks
Dr. Thomas E. Wade
General Chairman
University of South Florida

SESSION I - 8:15 A.M.
KEYNOTE ADDRESS
CMP CORPORATE OFFICERS:
"OUR COMPANY'S VISION FOR CMP IN THE FUTURE"

Richard J. Faubert
President and CEO
SPEEDFAM-IPEC

Jim Burke
CEO
R. HOWARD STRASBAUGH

Christopher Smith
Corp. VP
APPLIED MATERIALS

James W. Bagley
Chairman & CEO
LAM RESEARCH CORP

John Aldeborgh
President
EBARA AMERICA

FOLLOWED BY QUESTION & ANSWER SESSION
Moderator: Michael A. Martinez
MCA Corp.

SESSION II - 10 A.M. - 12 Noon
VLSI MULTILEVEL INTERCONNECTION
C.M.P. CONDUCTOR PROCESSES - Part I

Chairman: Dr. Duane Boning
MASS. INST. of TECH. (MIT)
Cambridge, Massachusetts

2.A "General Analysis of Dual-Step CMP for Copper Damascene Process" by K. Yang; ADVANCED MICRO DEVICES; Sunnyvale, CA. ........................................... 23 Invited Paper

2.B "CMP Processes for Noble Metals and Noble Metal Oxides" by G. Beitel, R. F. Schnabel, G. Mainka, A. Sanger and C. Dehm; INFINEON TECH; Munich, GERMANY; and R. Smali and Z. Chen; EKC TECH; Hayward, CA. ........................................... 33

2.C "Role of Alumina Phase and Size in Tungsten CMP" by D. Stein; SANDIA NAT'L LABS; Albuquerque, NM; and B. Her; FERRO; Penn Yan, N.Y. ........................................... 39
2.D "Fundamental Mechanisms in Metal CMP Using Model Slurries" by B. C. Lee, B. Wang, D. J. Duquette and R. J. Gutmann; RENSSELAER POLYTECH; Troy, N.Y. ............... 47

Invited Paper

2.E "Chemical Mechanical Planarization of Copper Interconnects Using Fixed Abrasive Polishing Pad" by V. Koinkar, R. Golzarian, Q. Luo, M. VanHanehem, J. Shen and P. Burke; RODEL; Newark, DE; and T. Fletcher, L.C. Hardy, J. Kollodge, J. Trice, T. Engfer and E. Funkenbusch; 3M CORP; St. Paul, MN. ............... 58

2.F "Hydroxy Radical Formation and Copper Line Corrosion in Cu-CMP" by J. Keleher, E. Tyre, S.V. Babu and Y. Li; CLARKSON UNIV; Potsdam, NY.; and R. Her; FERRO; Penn Yan, N.Y. ......................... 66

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2.G "Influence of Erosion and Dishing During Cu-CMP on Electrical Performance" by J. Grilliart, E. Vrancken, W. Fyen, M. Meuris and M. Heyns; IMEC; Kapeldreef, BELGIUM. ............... 75

2.H "Separation of Pad and Slurry Effects in Copper CMP" by D.R. Evans; SHARP LABS; Camas, WA; and M.R. Oliver and M.K. Ingram; RODEL; Newark, DE. ............... 79

2.I "Tungsten CMP Evaluation of Politex/IClOOO Pads Using Fe(NO3)2H2O Based Slurries With Oxide Buffing & Process Performance Optimization for 0.25 Micron Device Process" by P.K. Niu, P.T. Niu, C.F. Wen; WSMC; Taiwan, R.O.C. .................. 83

2.J "Copper CMP: The Role of Barrier Material and Its Effect on The Number of Polishing Steps" by D.A. Hansen, G. Moloney, M.E. Witty; CYBEQ NANO TECH; San Jose, CA. ............... 87

2.K "Robust Process Performance Window of Tungsten Chemical Mechanical Polish" by S.Y. Shih, L.H. Kuo, H.W. Chiu, Z.H. Lin and C. Hsia; ERSO/ITRI; Taiwan, R.O.C. .................. 91

SESSION III - 1:15 - 2:55 P.M.

VLsi MULTILEVEL INTERCONNECTION C.M.P. PROCESS CHARACTERIZATION

Chairman: Dr. Dale Hetherington
SANDIA NATIONAL LABS
Albuquerque, New Mexico

3.A "Integration of CMP Into a Low Volume, Fast Cycle Time 0.35 Micron CMOS ASIC Manufacturing Line" by K. Stribley, G. Hayward, M. Pult and D. Inman; MITEL SEMI; Plymouth, UNITED KINGDOM. ..................... 97

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3.B "Evolution of CMP Process Control Methodology for High Volume Manufacturing" by J. A. McKinnis, S.L. Lantz and D E. Sauer; INTER CORP; Hillsboro, OR. .................. 104

3.C "Production Status of 300mm CMP" by K. Ebner, P. Faustmann, W. Glashauser, D. Haggart, K. Herlitz and L. Teichgraber; INFINEON SC300; Dresden, GERMANY. ............... 112

3.D "Advanced Front End CMP and Integration Solutions" by R. Jin, S.H. Ko, B.A. Bonner, S. Li, T.H. Osterheld and K.A. Perry; APPLIED MATERIALS; Santa Clara, CA. .................. 119

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SESSION IV - 3:10 - 5:30 P.M.
VLSI MULTILEVEL INTERCONNECTION
C.M.P. SHALLOW TRENCH ISOLATION (STI)

Chairman: Dr. Peter Burke
RODEL INC
Newark, Delaware

4.A "Reverse Active Mask and CMP Over Polishing Impact on Shallow Trench Isolation for a 0.20 Micron Flash Memory* by P. Colpani, S. Ratti, A. Rebora and D. Berselli; ST MICRO; Agrate Brianza, ITALY. ........................................... 131
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4.B "Effects of a CMP Process on Within-Wafer STI Planarity" by Y. Wu, G. Brooks, T. Chamberlin and M. Lube; IBM MICRO; Essex Junction, VT. ........................................... 140

4.C "Ceria-Based slurries for STI Planarization* by S.V. Babu; CLARKSON UNIV; Potsdam, N.Y.; B. America; KODAK; and R. Srinivasan and Y.S. Her; FERRO; Penn Yan, N.Y............ 148
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4.D "Integration of STI Reverse Mask Effect and 520C Oxide-TEOS Based Oxide Film on STI CMP Process for the Sub-0.15 Micron DRAM* by T.H. Lee, W.P. Chang, T.C. Lin, H. L. Meng, O. Cheng, C. L. Kuo, K.C. Lin and S.C. Chien; UNITED MICRO CORP; Taiwan, R.O.C. ............................... 155


4.F "Design and Processing Considerations in a Production Worthy Shallow Trench Isolation Process" by R. Sehgal, S. Chadda, L. Prowell and G. Frazier; ATMEL CORP; Colorado Springs, CO. ............................... 169
Invited Paper

4.G "Dishing Reduction for STI-CMP by Inserting Polysilicon Buffer Layer* by V.S.K. Lim and W.L. Goh; NANYANG TECH UNIV; SINGAPORE; and F. Chen, A. See, C.H. Loh, C. Lin, Q.H. Zhong and M. Xin; CHARTER SEMI; SINGAPORE. ............................... 177

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4.H "Monitoring of Chemical-Mechanical Polishing Quality in Shallow Trench Isolation* by H.C. Chen, Y.T. Wei, M.S. Yang and V. Wang; UNITED MICRO CORP; Taiwan, R.O.C. 187

Friday, March 3, 2000
SESSION V - 8:00 - 9:40 A.M.
VLSI MULTILEVEL INTERCONNECTION
CMP MODELING & SIMULATION

Chairman: Dr. Bin Zhao
CONEXANT SYSTEMS
Newport Beach, California

5.A "Overview of Methods for Characterization of Pattern Dependencies in Copper CMP" by T. Park, T. Tugbawa and D. Boning; MASS. INST. of TECH; Cambridge, MA. .......... 197
Invited Paper

5.B "Influence of Microstructure and Mechanical Properties of Polishing Pads on CMP* by H. Liang, J. Lee; UNIV of ALASKA; Fairbanks, ALASKA. ........................................... 206
Invited Paper
5.C "Gradient and Radial Uniformity Control of a CMP Process Utilizing a Pre- and Post- Measurement Strategy" by J. Kim, Moyne, and C.E. Chemali; UNIV MICHIGAN, Ann Arbor, MI. 215

5.D "CMP Pad Displacement and Slurry Flow Characteristics: Finite Element Analysis" by J.A. Tichy, C.J. Clutz and T.S. Cale; RENSSELAER POLYTECH; Troy, N.Y. 222

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5.E "Characterization of Endpoint and Wafer Level Non-Uniformity Using In-Situ Thermography" by D. White, D. Boning, A. Gower; MASS INST of TECH; Cambridge, MA... 229

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5.F "A Plasticity Based Model for Material Removal During Chemical Mechanical Polishing" by A. Chandra and G. Fu; IOWA STATE UNIV; Ames, IA; S. Guha; SPEEDFAM-IPEC; Chandler, AZ; and G. Subhash; MICHIGAN TECH UNIV; Houghton, MI. 239

5.G "Oxide Polishing Kinetics - Physical Based Modeling" by V. Sukharev and J. Pallinti, LSI LOGIC; Santa Clara, CA. 243

5.H "Effect of Wafer Edge Contact Stress on Non-Uniformity During CMP" by C.C. He, C.Y. Chiou, W. C. Pan, H.L. Chung; CHUNG-SHAH INST of SCI & TECH; Taiwan, R.O.C. 247

5.I "Controlling CMP Removal Rate Profiles Using Empirical Modelling" by A. Jensen, J. Farber and P. Renteln; LAM RES CORP; San Jose, CA. 251

5.J "Using Smart Dummy Fill and Selective Reverse Etchback for Pattern Density Equalization" by B. Lee, B. Boning; MIT; Cambridge, MA; and D. Hetherington and D. J. Stein; SANDIA NAT'L LABS; Albuquerque, NM. 255

5.K "A New Model by Product Effective Polish Rate for Oxide CMP APC System" by J. Y. Lin, J.I. Wu and C.F. Lin; UNITED MICRO CORP; Taiwan, R.O.C. 259

SESSION VI - 9:50 - 11:30 A.M.
VLSI MULTILEVEL INTERCONNECTION
CMP CONSUMABLES

Chairman: Dr. Frank B. Kaufman
CABOT CORP.
Aurora, Illinois

6.A "STI CMP Using Fixed Abrasive - Demands, Measurement Methods and Results" by A. Romer, P. Thieme and M. Hollatz; INFINEON; Dresden, GERMANY; and T. Donohue; APPLIED MATERIALS; Santa Clara, CA; and J. Gagliardi; 3M LABS; St. Paul, MN; F. Weimar; 3M LABS; Neuss, GERMANY. 265

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6.B "Viscoelastic Behavior of Polishing Pad and Its Influence on Polishing Non-Uniformity" by H.J. Kim, H. Y. Kim and H. D Jeong; PUSAN UNIV; Pusan, SOUTH KOREA. 275

6.C "Treatment of CMP Wastes" by S. Raghavan, Y. Sun and W. Huang; UNIV ARIZONA; Tucson, AZ. 283

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6.D "Pad Life Optimization by Characterization of a Fundamental Pad-Disk Interaction Property" by G. Prabhu, S. Kumaraswamy and D. Flynn; APPLIED MAT'L; Santa Clara, CA; and S. Qamar and T. Namola; ABRASIVE TECH; Westerville, OH. 293

6.E "4th Generation W Slurry for Plug and Damascene Applications" by M Peterson, B. Tredinnick and R. Small; EKC TECH; Hayward, CA. 300

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6.F "CMP Wastewater Treatment" by J.H. Golden; MICRO-BAR; Sunnyvale, CA.

6.G "Pad Surface Roughness After Conditioning in CMP" by C.T. Wang, W. Jeng and C.C. Liang; ASIA IC MIC; Taiwan, R.O.C.; L.K. Chou and R. Chen; WINBOND; Taiwan, R.O.C

6.H "CMP of TaSiN Barrier for Stack Capacitors" by L. Economikos and F. F. Jamai; IBM/INFINEON ALLIANCE; Hopewell Jct., N.Y.

6.I "A Novel Disk and Its Performance in Pad Conditioning of W CMP" by T.C. Wang, T.E. Hsieh; NAT'L CHIAO-TUNG UNIV; Taiwan, R.O.C.; Y.L. Wang; TAIWAN SEMI; Taiwan, R.O.C.; K. Yang, W. Pan; APPLIED MAT'L; Taiwan, R.O.C.; and J. Sung; KINIK CO; Taiwan, R.O.C.

6.J "Point-of-Use Filtration Lifetime for CMP Slurries" by C. Lee, M. Federau, D. Ligocki, T. Myers and S. Lesiak; CABOT; Aurora, IL.


6.L "Diagnostic and Prediction of Pad Life in CMP" by C.T. Wang, W. Jeng; ASIA IC; Taiwan, R.O.C.; and C.Y. Huang; WINBOND; Taiwan, R.O.C.

6.M "Bond Strength and Crystal Retention Properties of CMP Pad Conditioners Manufactured With P.B.S. Brazed Crystal Bonding Vs Electroplated Crystal Bonding Technologies" by T. Namola and S. Qamar; ABRASIVE TECH; Westerville, OH.

6.N "Defect Evaluation for Fixed Abrasive CMP" by K. Mikhaylich and M. Ravkin; LAM RES; Fremont, CA.

6.O "Enhancement of Padlife on Orbital Tools Through Uniform Pad Conditioning" by D. Potter and I. Golkar; SPEEDPAM IPEC; Chandler, AZ.

SESSION VII - 11:30 A.M. - 12:30 P.M.
VLSI MULTILEVEL INTERCONNECTION
Dedicated Time For CMP PAPERs, EXHIBIT VIEWING

SESSION VIII - 1:45 - 3:25 P.M.
VLSI MULTILEVEL INTERCONNECTION
C.M.P. DIELECTRIC PROCESSES
Chairman: Dr. Paul Feeney
CABOT CORP.
Aurora, Illinois

8.A "Oxide CMP: Planarization Performance Upon Different Integration Schemes" by E. Perrin, M. Rivoire, A. Inard, M. Jouty; S T MICRO; Crolles, FRANCE; J. Van Hassel; PHILIPS; J.C. Oberlin; CNET; Meylan, FRANCE.
8. B "Improving Within-Die Nonuniformity in Dielectric CMP* by T. Smith; SKW; Fremont, CA; S. Fang, G. Shinn, J. Stefani, Z. Tang, S. Chang, S. Garza and J. Campbell; TEXAS INSTRUMENTS; Dallas, TX; D. Boning; MIT; Cambridge, MA ................................................................. 362

8. C "CMP of Various Low-k Dielectrics" by F. Zhang, P. Galvez, S.P. Mukherjee, L. Forester and S.Q. Wang; HONEYWELL; Sunnyvale, CA ................................................................. 365

8. D "Total Planarization of the MIT 961 Mask Set Wafers Coated With HDP Oxide" by J.J. Gaglardi; 3M CO; St. Paul, MN and T. Vo; RODEL; Sunnyvale, CA ................................................................. 373 Invited Paper

8. E "The CMP Process of Polyimide for Low-k Dielectric Application in ULSI Multilevel Interconnection" by Y.L. Tai and Y.L. Wang; TSMC; Taiwan, R.O.C ................................................................. 379

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8. F "FSG-CMP Process Development & Characterization for 0.18 Micron Technology & Beyond" by L.S. Leong, F. Chen, F.L. Chin, C. H. Loh, C. Lin and A. Cuthbertson; CHARTER SEMI MFG; SINGAPORE; V. Lim; NANYANG TECH UNIV. and D. Lim; NAT'L UNIV of SINGAPORE; SINGAPORE ................................. 387

8. G "Defect Reduction for ILD CMP" by A. Francis, P. Feeney, G. Bogush and F. Khan; CABOT; Aurora, IL ................................................................. 391


8. I "Optimizing Dielectric CMP Planarization Processes" by D.L. Hetherington, D.J. Stein; SANDIA LABS, Albuquerque, NM; and M.R. Oliver; RODEL; Newark, DE ................................................................. 399

8. J "Characterization of an Oxide CMP Polishing System Containing an Independently Controlled Guide Ring" by K.G. Pierce, R. Schgal, S. Chadda; ATMEL; Colorado Springs, CO ................................................................. 403


8. L "Characterizing an ILD CMP Process Using Colloidal Silica Slurry to Achieve a Longer Pad Life" by P. Chavez; INTEGRATED DEVICE TECH; Salinas, CA; and A. J. Clark; RODEL; Phoenix, AZ ................................................................. 413

8. M "Optimization of Polishing Pad Profile and Its Effect on 300 mm Oxide CMP Process" by H.M. Wang, G. Moloney and S. DeGuzman; CYBEQ NANO TECH; San Jose, CA ................................................................. 417


SESSION IX - 3:25 - 4:45 P.M. VLSI MULTILEVEL INTERCONNECTION C.M.P. NOVEL APPLICATIONS

Chairman: Dr. Michael A. Fury SILTERRA SDN. Kulim, Malaysia

9. A "A Novel High-Frequency Quasi-SOI Power MOSFET Using a CMP Technology" by A. Matsumoto, Y. Hiraoaka, T. Sakai and T. Yachi; NTT RES. LABS; Tokyo, JAPAN ................................................................. 427 Invited Paper
9.B "Chemical Mechanical Planarization of Thin Film Read/Write Heads" by E. Lee, F. Martin, F. Eschbach, J. Ortega, B. Phipps; IBM Almaden Res. Ctr; San Jose, CA. Invited Paper

9.C "Atomically Flat Surface of Compound Semiconductors by Chemical-Mechanical Polishing" by P.S. Dutta and R.J. Gutmann; RENSSELAER POLYTECH INST; Troy, N.Y. Invited Paper

9.D "Applications of CMP in the Thin Film Magnetic Head Fabrication" by D.S. Zhou; READ-RITE CORP; Fremont, CA. Invited Paper

SESSION X - 4:45 - 6:00 P.M.
VLSI MULTILEVEL INTERCONNECTION
C.M.P. CONDUCTOR SYSTEM - Part II

Chairman: Dr. Kathleen Perry
OBSIDIAN INC
Fremont, California

10.A "Annealed Properties of Electroplated Cu Thin Film and Their Effect on CMP" by I. Ivanov and C.H. Ting; CUTEK RES; San Jose, CA. Invited Paper

10.B "Investigation of Aluminum CMP to Apply to Sub-Quarter Micron DRAM Devices" by J.Y. Kim, C.H. Jeong, N.H. Park, S.B. Han, J. W. Park; HYUNDAI; Cheongju, KOREA; and J. J. Kim; SEOUL NAT'L UNIV; Seoul, KOREA.


- POSTER PAPERS -

10.E "Dual Damascene Tungsten Process for the Bit Line Application of DRAMs" by Y.A. Cho, W.H. Jin, W.J. Lee and I. Hong; HYUNDAI; Cheongju, KOREA; and S.K. Rha; TAEJON NAT'L UNIV; Taejon, KOREA.

10.F "IR Thermal Mapping of Process Variations at Cu-CMP" by Z.H. Lin, H.W. Chiou, S.Y. Shih and C. Hsia; ERSO/ITRI; Taiwan, R.O.C.

10.G "Integration Methodology of W CMP Process for Sub-0.18 Micron Process Applications" by Y.L. Wang, J. Wu, T.C. Wang, J.K. Lan, Y.L. Cheng and J. Dun; TSMC; Taiwan, R.O.C.

10.H "Polish Behavior of Tungsten Plug Planarization" by Z.H. Lin, H.W. Chiou, S.Y. Shih and C. Hsia; ERSO/ITRI; Taiwan, R.O.C.

SESSION XI
VLSI MULTILEVEL INTERCONNECTION
C.M.P. CLEANING PROCESSES

- POSTER PAPERS -

11.A "Discussion and Simulation of Various CMP Scratch Issues" by E. Tseng; UNITED MICRO CORP; Taiwan, R.O.C.

SESSION XII
VLSI MULTILEVEL INTERCONNECTION
C.M.P. INSTRUMENTATION & HARDWARE
- POSTER PAPERS -

12.A "All Optical Metrology for Characterizing CMP of Copper Damascene Structures" by M. Banet, M. Joffe, M. Gostein, A. Maznev, C. Moore and R. Sacco; PHILIPS ANALYTIC; Natick, MA .......................... 537

12.B "Improvement of Chemical Mechanical Polishing Characteristics By Using Nozzle Type Injector" by K.J. Kim, S.T Moon and H.D. Jeong; PUSAN UNIV; Pusan, KOREA ......................... 541

12.C "Automatic Analysis and Control of Hydrogen Peroxide Concentration in Copper and Tungsten Polishing CMP Slurry" by K. Nicholes, T. Lemke, J. Bare, B. Johl; BOC EDWARDS; Santa Clara, CA .................................................. 545

12.D "Advanced In-Line Monitoring of Metal Residual and Dielectric Loss at Cu-CMP" by Z.H. Lin, H.W. Chiou, S.Y Shih and C.Hsia; ERSO/ITRI; Taiwan, R.O.C.; and H Rotenberg; NOVA INST; Taiwan, R.O.C ............................................. 550

12.E "On-Line Measurement of Oxide Erosion, Metal Residuals and Field Oxide Thinning in Copper CMP Processing" by B. Srinivasan and F. Stanke; SENSYS INST; Santa Clara, CA ........................................... 554

12.F "Process Control and Endpoint Detection With Fullscan ISRM System in Chemical Mechanical Polishing of Cu Layer" by B.W. Adams, B. Swedek, R. Bajaj, K. Wijekoon, S. Nanjangud, A. Wiswesser, S. Tsai, D.A. Chan, F. Redeker and M. Birang; APPLIED MAT'L; Santa Clara, CA ........................................... 558


12.H "An Improvement of Oxide CMP Process Performance Through the Head Design" by H.M. Wang, G. Moloney, M. Stella and S. DeGuzman; CYBEQ NANO TECH; San Jose, CA ........................................ 566

12.I "Comparison of Instruments Used for Measuring Concentrations of Large Particles (> 1 Micron) in CMP Slurry" by M.R. Litchy, K. Nicholes and D.C. Grant; BOC EDWARDS; Chaska, MN. .................................................. 570