"Flip-Chip & Chip Scale Europe 2000"

-Flip-Chip Technologie
-HDI Micro Via Leiterplatten
-Chip Scale Packaging Technologien
-Anwendungen für Chip Scale Packaging
-Vom CSP zum Waferlevel CSP
-Materialien für CSP-Herstellung
-Bestückungstechnik
-Innovationen
-Qualitätssicherung und Test

-Flip-Chip Technology
-High Density Interconnect Micro Via Printed Circuit Boards
-Chip Scale Packaging Technologies
-Applications for Chip Scale Packaging
-From CSP to Waferlevel CSP
-Materials for Manufacturing CSP’s
-Assembly Technology
-Innovations
-Quality Assurance and Test


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### Flip-Chip-Technology

1. **Multi-Flip-Chip-Modules on Silicon Substrates without Redistribution and Underfill**
   Dipl.-Ing. Hans-Wolfgang Diesing, Strand Interconnect AB

2. **Ordered Particles – the revolution for flip chip assembly?**
   Dipl.-Ing. Christian Ellsäßer, Loctite European Group, Garching

3. **Is flip chip production possible without underfilling?**
   Dipl.-Ing. Michael Läntzsch, Litton-Kester-Solder GmbH, Gernlinden

4. **Flip Chip Interconnections with Anisotropic Conductive Adhesives**
   Dipl.-Ing. Ralf Miessner, Fraunhofer-Institut, Berlin

### High Density Interconnect & Micro Via Printed Circuit Boards

5. **Base Materials for HDI-Applications**
   Dr. Manfred Cygon, ISOLA AG, Düren

6. **Technologies for Microvia PCB's and CSP substrates**
   Dr. Thomas Kreutz, Photo Print Electronic, Schopfheim

7. **New Manufacturing Concepts for HDI Substrates**
   Dr. Walter Schmidt, Dyconex AG, CH-Zürich

### Chip-Scale Packaging Technologies

8. **Wafer Level Packaging – A Worldwide Review and Future Outlook**
   Mike Campbell, BPA (Europe) Ltd., United Kingdom

9. **Low Cost Bumping and Wafer Level CSP using Electroless Plating and Leadfree Solder**
   Dr. Elke Zakel, PacTech, Nauen

### Chip Scale Packaging Application

10. **Wafer Level Packaging for Imaging and light detection applications**
    Tami Mazel, Moshe Kriman, Shellcase, Jerusalem/ISRAEL

11. **Qualification of CSP's for automotive environments**
    Dr. Günter Lugert, SIEMENS Automotive, Regensburg
From CSP to Waferlevel CSP

„A survey of CSP- and waferlevel CSP-Solutions“
Dipl.-Ing. Hans-Jürgen Hacke, SIEMENS AG, München

„Reliable and Low Cost Wafer Level Packaging“
Vern Solberg, Tessera Inc., CA / U.S.A.

Materials for Manufacturing CSP’s

„Silicone Materials for CSP recent developments“
Dr. Eric Vanlathem, Dow Corning

„The Key Role of Dielectric Materials to Match the Needs of CSP, Flip Chip and HDI or other Advanced Interconnect Solutions“
Dr. Martin Meier, Mr. Albert Achen, The Dow Chemical Company, CH-Horgen

„Lead free Solder for CSP“
Vern Solberg, Tessera Inc., CA / U.S.A.

Assembly Technologies

„An integrated solution for placement of Flip Chip devices into High-Density Substrates“
Robert Peter, Alphasem AG, CH-Berg

Innovations

„New IC Package Generation: PSGA“
Dipl.-Ing. Joachim Krause, SIEMENS AG, Bruchsal

„Snap Array CSP – Ceramic CSP’s for High Performance and High Reliability Applications“
Seigo Matsuzono, Takaharu Uratsuka, Kyocera, Japan

„FPBGA for Memory Components“
Günther Rauschert, Advanced Micro Devices, München

„Triple-Chip-Stacked-CSP“
Naoyuki Tajima, Sharp Electronics Europe GmbH, Hamburg

Quality Assurance and Test

„3-D Bumped Wafer Inspection System for CSP & Flip-Chip packaged IC’s“
Dipl.-Ing. Thomas Trenkler, Digital Instruments, Mannheim

„X-Ray Inspection Applications for Chip Scale Packages“
Dino Franz, Macrotron, Kirchheim bei München