1989 VIRGINIA POWER ELECTRONICS CENTER SEMINAR

VPEC INDUSTRY-UNIVERSITY PARTNERSHIP PROGRAM

SEPTEMBER 25-27, 1989

PURPOSE

The seminar provides a forum for engineers and researchers from industry, government, and the university to exchange ideas, promote advanced concepts in research and its applications, and to encourage cooperative R&D programs in power electronics.

Sponsored by

Virginia Power Electronics Center
Department of Electrical Engineering
Virginia Polytechnic Institute and State University
340 Whittemore Hall
Blacksburg, Virginia 24061
(703) 231-4536
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TUTORIAL: UNIFIED SWITCH MODEL AND CURRENT MODEL CONTROL
Chairman: Dr. F.C. Lee

1. SIMPLIFIED ANALYSIS OF PWM CONVERTERS USING THE MODEL OF THE PWM SWITCH PART I: CONTINUOUS CONDUCTION MODE
V. Vorperiam

A circuit-oriented approach to the analysis of PWM converters is presented. This method relies on the identification of a three-terminal nonlinear device, called the PWM switch, which consists of only the active and passive switches in a PWM converter. Once the invariant properties of the PWM switch are determined, an average equivalent circuit model for it can be derived. The DC and small-signal characteristics of a large class of PWM converters can then be obtained by a simple substitution of the PWM switch with its equivalent circuit model.

1.2 DC ANALYSIS AND DESIGN OF ZERO-VOLTAGE-SWITCHED MULTI-RESONANT CONVERTERS
W. Tabisz and F.C. Lee

Recently introduced multi-resonant converters (MRCs) provide zero-voltage-switching (ZVS) of both active and passive switches and offer a substantial reduction of transistor voltage stress and an increase of load range, compared to their quasi-resonant converter counterparts. Employing the resonant switch concept, a simple, generalized analysis of ZVS MRCs is presented. The conversion-ratio and voltage stress characteristics are derived for basic ZVS MRCs. Based on analysis, a design procedure which optimizes the selection of resonant elements for maximum conversion efficiency, is proposed.

SESSION I
DESIGN AND ANALYSIS OF MULTI-RESONANT CONVERTERS
Chairman: R. Ridley

1.1 HIGH-FREQUENCY FORWARD ZVS-MRC FOR A LOW-PROFILE HIGH-DENSITY ON-BOARD POWER SUPPLY
W. Tabisz and F.C. Lee

A forward zero-voltage-switched multi-resonant converter is used to implement a high-density (50W/in'), low-profile (1.85 in) on-board power supply for VIISIC applications. Switching above 2 MHz, the converter operates with 40-60 V input voltage range and delivers 5 V/10 A output. A prototype has been developed using low-profile magnetics and thick-film hybrid technique.

1.3 DC ANALYSIS AND DESIGN OF FORWARD ZVS-MRC
W. Tang, W. Tabisz, V. Vorperiam and F.C. Lee

A dc analysis of the forward ZVS-MRC is presented. A computer program is used to generate dc conversion ratio, voltage and current stress, and magnetizing current characteristics. Design guidelines for the forward ZVS-MRC are presented and the results of the analysis are compared with SPICR simulation and experiments.

1.4 POWER-HYBRID DESIGN OF A HIGH-FREQUENCY ZVS-MRC

Thick-film-hybrid technology is used to fabricate a half-bridge, half-wave, zero-voltage-switched multi-resonant converter for 150-350 Vdc off-line application. With a conversion frequency of 4-10 MHz, the converter delivers 100 W at 5 V output with a 75% efficiency at an input voltage of 300 Vdc and a power density of 33W/in'. This paper presents detailed electrical design, hybrid processing, and thermal considerations.
The multi-resonant switch is modified to provide constant-frequency operation of ZVS-MRCs. The paper describes the proposed constant-frequency multi-resonant switch and its application in generating the family of constant-frequency (CF) ZVS-MRCs. Experimental designs and performances of several CF ZVS-MRC topologies are also presented.

1.6 NONLINEAR DESIGN OPTIMIZATION OF QUASI-RESONANT CONVERTERS

A. Lotfi and F.C. Lee

A nonlinear optimization procedure previously used for PWM converter design is extended and applied to quasi-resonant converters (QRCs). Design equations, operational constraints and an objective function are presented for QRCs. The routine is used to compare weights and efficiencies of optimally designed QRCs and their PWM counterparts, giving insight into the limitations of each topology and its applicability to a given set of specifications.

SESSION II

ZERO-VOLTAGE-SWITCHING TECHNIQUES

Chairman: Dr. D.Y. Chen

2.1 COMPARISON OF HALF-BRIDGE, ZCS-QRC AND ZVS-MRC FOR OFF-LINE APPLICATIONS

M. M. Jovanovic, R. Farrington and F.C. Lee

Performance of the half-bridge (HB) zero-current-switched (ZCS) quasi-resonant (QR) and zero-voltage switched (ZVS) multi-resonant (MR) converters are compared with respect to their efficiency, input voltage range, semiconductor stresses, power density, and reliability. The efficiency of the HB ZVS-MRC at a given nominal input is shown to be highly dependant on the range of the input-voltage. The efficiency suffers when the converter has to be designed to cover a wide range. However, this is not the case for the HB ZCS-QRC.

2.2 ZERO-VOLTAGE-SWITCHING WITH FIXED-FREQUENCY CLAMPED-MODE RESONANT CONVERTERS

J. A. Sabate and F.C. Lee

Clamped-mode resonant converters (CMRC) operated at fixed-frequency above resonant frequency offer zero-voltage-switching for all active devices. The series CMRC can operate with zero-voltage-switching only for a reduced load range and the parallel CMRC offers zero-voltage-switching from no load to full load. The paper presents the design of a prototype for an off-line application for series and parallel realizations. Analysis of the breadboard implementation of each design permits the evaluation of the main sources of loss, as well as a comparison of both alternatives. Zero voltage switching minimizes loss and stress in the components for the required full bridge topology. Also the internal diodes of the MOSFETs can be used, reducing the component count.

2.3 THE OPERATION OF A FULL-BRIDGE ZERO-VOLTAGE-SWITCHED PWM CONVERTER

D. Sable

The operation of a full-bridge zero-voltage-switched PWM converter is detailed. It is shown how proper design of the transformer leakage inductance and magnetizing inductance can ensure zero-voltage-switching over a full range of line and load conditions. The converter is compared with a standard full-bridge PWM converter for use in high power, low voltage applications.

SESSION III

POWER-FACTOR CORRECTION

Chairman: Dr. V. Vorperian

3.1 DESIGN AND ANALYSIS OF AN ACTIVE UNITY POWER FACTOR CORRECTION CIRCUIT

C. Zhou, R. Ridley and F.C. Lee

The design of a boost topology active unity power-factor correction circuit with hysteresis control for off-line switching power supply is described in detail. A computer-aided design program is developed to give optimal components selection. Simulation and experimental results are presented.

3.2 AVERAGE SMALL-SIGNAL MODEL OF BOOST POWER FACTOR CORRECTION CIRCUIT

R. Ridley

A three-terminal, small-signal model for the boost power-factor correction circuit is developed. The model is applicable for frequencies below the line frequency, and is useful for designing the low-frequency compensation network for feedback of the output voltage.

3.3 THE SIMULATION OF SWITCHING CONVERTERS USING THE NEW VERSION COSMIR PROGRAM

C. Hsiao, R. Ridley, and F.C. Lee

This paper describes a new version of the simulation program COSMIR. Using a switch-driven instead of a mode-driven algorithm, COSMIR operates with a much simplified user input and is capable of simulation of more complex circuits such as power-factor correction circuit, parallel converters and multi-resonant converters.

WEDNESDAY, SEPT. 27

SESSION IV

HIGH DENSITY DISTRIBUTED POWER SUPPLY TECHNOLOGIES

4.1 HIGH DENSITY DISTRIBUTED POWER SUPPLY TECHNOLOGIES

This is a special session dedicated to the high density board-mount power supply
development effort for VIISIC applications. All work is sponsored by Wright Patterson Air Force Base, Dayton, Ohio.

Chairman: Richard Strawser, Research and Development Center, Wright Patterson Air Force Base

4.2 ADVANCED LOW VOLTAGE POWER MOSFETS FOR EFFICIENT SYNCHRONOUS RECTIFICATION

Charles Korman, GE Corp. R&D Center

A novel power DMOSFET technology has been developed which allows both low specific input capacitance and low specific on-state resistance to be achieved at the same time. Under an Air Force funded program, 30 and 50 volt devices have been developed based upon this technology. These devices have an on-state resistance of 5 and 9 milliohms, respectively, along with ohm-pf ratings of 10 and 20, and are ideal for use as synchronous rectifiers in high density power converter applications requiring operation at frequencies in the 1-8 MHz range.

SESSION V

DISTRIBUTED POWER SYSTEMS

Chairman: Dr. B. Cho

5.1 DESIGN CONSIDERATIONS FOR DISTRIBUTED POWER SYSTEMS

Q. Liu, S. Schultz, B. Cho, and F.C. Lee

Distributed power systems are generally composed of cascaded stages of parallel switching regulators. System design requires the interfacing of regulators and filters to meet certain specifications while avoiding unwanted interactions. Input filters are designed for a two-stage conversion topology to minimize bus interaction and degradation of loop gains. Based on small-signal results, subsystem and integrated system performance are predicted.

5.2 LARGE SIGNAL MODELING AND SIMULATION OF DISTRIBUTED POWER SYSTEMS

S. Schultz, Q. Liu, B. Cho, and F.C. Lee

Large-signal simulation of complex power conversion systems has become a viable tool for system development. The modeling of multiple-stage distributed power systems is discussed. Modularity and parallelability are stressed for convenience and versatility in the construction of large system models. The large-signal results are shown to be quite useful in design, performance analysis and failure-mode operation studies.

SESSION VI

SPACE STATION POWER SYSTEM

Chairman: Dr. B. Cho

6.1 MODELING AND SIMULATION OF SPACE STATION POWER SYSTEM

J.R. Lee, I.S. Tsai, S.J. Kim, A. Patil, B. Cho and F.C. Lee

The power system of a space station is modeled and simulated using EASYS software. The system consists of a sequential shunting solar array, battery, battery charger/discharger, driver inverter, and loads. The performance of the system is investigated under different operating conditions including sunlight mode, eclipse mode, and transition mode. Also, possible failure operations in each operating mode are discussed.

6.2 A SIMPLE SCHEME FOR UNITY POWER-FACTOR RECTIFICATION FOR HIGH-FREQUENCY AC BUSES

V. Vorperian and R. Ridley
A simple scheme is proposed for off-line unity power factor rectification for high-frequency ac buses (20 kHz), such as those implemented on the space station. In this scheme, a bandpass filter of the series resonant type centered at the line frequency is inserted between the line and the full-wave rectified load. The $Q = Z_0/R_L$ formed by the load and the characteristic impedance of the tank circuit determines the power factor, peak stresses and the transient response of the rectifier.

SESSION VII

POWER DEVICES

Chairman: Dr. M.M. Jovanovic

7.1 RBSOA CHARACTERIZATION OF GTO DEVICES

G. Carpenter, F.C. Lee and D.Y. Chen

GTO device technology has made tremendous progress in the past ten years. The devices have been proven reliable and a wide variety are currently made commercially available. GTO technology has found applications in the areas of high-power uninterruptible power supplies and industrial motor drives. However, the manufacturers' data sheets provide little information about reverse bias safe operating area (RBSOA). This, perhaps, is due to the difficulties of making a nondestructive measurement of GTO RBSOA. This paper summarizes the results obtained in the investigation and evaluation of GTO RBSOA. In the paper, a GTO RBSOA tester is first described. The approach taken to characterize the RBSOA of a GTO is then discussed. This approach is very different from that used in a BJT RBSOA characterization. The results obtained from testing several commercial GTO devices will be summarized.

7.2 POWER TESTS OF FERRITE MATERIALS IN 1 TO 20 MHZ FREQUENCY RANGE

P. Gradzki and F.C. Lee

A simple and fast core loss measurement method is described. An impedance analyzer is used to obtain core loss and normalized equivalent parallel resistance which represents the power loss of the material. Large signal measurements are possible due to the use of high-frequency power amplifiers and specially designed test fixtures which attenuate current and voltage 50 times with $\pm 0.5\degree$ phase and $\pm 1\%$ magnitude error below 20 MHz.

7.3 A SIMPLE MODEL PREDICTS SMALL-SIGNAL CONTROL LOOP BEHAVIOR OF MAGAMP POST REGULATOR

D. Y. Chen, J. Lee, and C. Jamerson

This is a continuation of a paper by Cliff Jamerson which was presented at the 1987 High Frequency Power Conversion Conference. That paper introduced a simple block diagram approach to describe two commonly used magamp reset circuits, the Type A and Type B. This analysis reveals resonant frequency shifting phenomenon inherent in Type A circuit. A procedure for calculating the gain and loop pole in the control loop of each reset is given. The procedure also shows how to compensate the error amplifier for stable operation.

7.4 MAGAMP POST REGULATORS - PRACTICAL DESIGN CONSIDERATIONS TO ALLOW OPERATION UNDER EXTREME LOADING CONDITIONS

J. Lee, D. Y. Chen, and C. Jamerson

This paper establishes practical design equations and guidelines to allow magamp operation under extreme loading conditions. Three conditions are considered: shutdown of output, foldback of the output current, and operation under discontinuous inductor current mode.