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**Liability Issues Associated with Electrical Overstress in Computer Hardware, Design and Manufacture**

T.G. Mahn, Bell, Boyd & Lloyd

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**Session Moderator:** Ted Dangelmayer, AT&T Technologies

### Estimating ESD Losses in the Complex Organization

S.A. Halperin, Stephen Halperin & Associates

### A "Tailorable" ESD Control Program for the Manufacturing Environment

N.B. Fuqua, IIT Research Institute

### Internal Quality Auditing and ESD Control

D.A. Smith and C.D. Rief, NCR Comten, Inc.

### The Physics of Charge Neutralization by Air Ions

N. Jonassen, Technical University of Denmark

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**Session Moderator:** Timothy J. Maloney, Intel

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D. Scott, J. Hall and G. Giles, Texas Instruments

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W.J. Orvis, J.H. Yee and G.H. Khanaka, Lawrence Livermore National Laboratory

### Avoiding Thermal Breakdown in Overdriven Digital Circuit Outputs

R.L. Swent, Schlumberger Palo Alto Research

### Sheet Resistance Measurement of Buried Shielding Layers

B.A. Unger, R.G. Chemelli and D.L. Hart, Bell Communications Research

### The Probability of an ESD Failure in an Unprotected Environment

J. Giusti, Storage Technology

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**Session Moderator:** Jerry Soden, Sandia National Laboratories

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R.E. McKeighen, W. Daily, T. Pang, P. Huynh, J. Wittman and B. Wiley, Motorola/GEG
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R.G. Taylor and J. Woodhouse, British Telecom

Computer Simulation of ESD and Lightning Events
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Triboelectric Charging of Personnel From Walking on Tile Floors
E.W. Chase and B.A. Unger, Bell Communications Research

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B.N. Stevens, Dow Chemical Company

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R.H. Gompf, Consultant to NASA

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The workshop will address resistivity, static decay and charge generation testing on floors, work surfaces, shipping tubes and other ESD control materials.

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Chair: Ted Dangelmayer, AT&T Technologies, and Stephen Halperin, Stephen Halperin & Associates

Discussion will focus on the key elements of ESD control. Topics will include economic analysis, managerial commitments, auditing and training programs, design and management, and practical application of static control theory.

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The workshop will focus on processing and device structure, circuit and layout considerations, testing, university research and the education of the next generation of designers.

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