TECHNICAL CONTENTS

Session Ia: Plenary Invited Papers

Ia1
Physics and Technology for MOSFETs at 0.1 micron and below
D. ANTONIADIS

Ia2
Photonic Integrated Circuits
A. CARENCO

Session Iia: Modelling of silicon and compound semiconductor devices

Iia1
Can cellular automata methods compete with Monte Carlo semiconductor device simulations? (invited)
G.ZANDLER, A.REIN, M.SARANITI, P.VOGL, P.LUGLI

Iia2
An analytical model of current-splitting in CMOS-compatible lateral bipolar transistors
D.FREUND, A.KLOES, A.KOSTKA

Iia3
Analysis and modeling of small-geometry effects on maximum cutoff frequency fT and forward transit time in high-speed self-aligned bipolar transistors
N.RINALDI, P.SPIRITO

Session Iib: Noise

Iib1
Low frequency noise in partially depleted SOI twin-MOSFET's
E.SIMOEN, C.CLAEYS
IIb2
Random telegraph signal related low-frequency noise peaks in submicrometer Si MOST's
E.SIMOEN, B.DIERICKX, C.CLAEYS

IIb3
Noise performance of MESFETs and MODFETs: influence of the gate leakage current
F.DANNEVILLE, G.DAMBRINE, H.HAPPY, A.CAPPY

IIb4
Low-frequency noise and microwave noise parameters in Si/SiGe heterojunction bipolar transistors
R.PLANA, H.KIBBEL, A.GRUHLE, L.ESCOTTE, J.P.ROUX, J.GRAFFEUIL

Session IIc: Thin Film Transistors and Special Devices

IIc1
Polysilicon thin film transistor: a study of some techniques of realisation of the channel region and of the gate
E.SCHEID, E.CAMPO, J.J.PEDROVIEJO, S.NAÎMI, G.SARRABAYROUSE, D.BIELLE-DASPET

IIc2
Analysis of hot carrier induced degradation in polycrystalline silicon thin film transistors
G.FORTUNATO, A.PECORA, G.TALLARIDA, L.MARIUCCI, M.VALDINOCI, A.GNUDI

IIc3
Large area deposition of device quality SiO₂ for poly Si TFT fabrication

IIc4
On the way to the Silicon carbide IMPATT
K.VASSILEVSKI, V.A.DMITRIEV, A.V.ZORENKO

Session IIIa: Plenary Invited Paper

IIIa1
The role of TCAD in Parasitic Analysis of ICs
R.W.DUTTON
Session IVa: Reliability and Testing

IVa1
Mechanisms of hot-carrier degradation of analog device parameters in n-MOSFETs
R. THEWES, W. WEBER, K. GOSER

85

IVa2
Study of process-induced mechanical stresses in multi-chip modules packaged with a chip-on-board technology
L. GUERIN, A. WEBER, P. SARBACH, M. DUOTOIT, P. CLOT

89

IVa3
Efficient calculation of 3-D stress distributions in silicon around embedded structures
R. SLEHOBIR, G. HOBLER, H. POTZL

93

IVa4
Generation of MOS model parameters covering statistical process variations
J. POWER, B. DONNELLAN, K. BURKE, K. MOLONEY, A. MATHEWSON, W. A. LANE

97

Session IVb: Noise

IVb1
Analysis and modeling of low frequency noise in extremely deep submicron silicon CMOS devices
O. ROUX-dit-BUISSON, G. GHIBAUDO, J. BRINI, G. GUEGAN

103

IVb2
Low-frequency noise sources in polysilicon emitter bipolar transistors: influence of hot-electron-induced degradation and post-stress recovery
A. MOUNIB, F. BALESTRA, N. MATHIEU, J. BRINI, G. GHIBAUDO, A. CHOVET, A. CHANTRE, A. NOUAILHAT

107

IVb3
Low-frequency noise in SOI MOSFET's from room to liquid helium temperature: experimental and numerical simulation results
J. JOMAHH, F. BALESTRA, G. GHIBAUDO

111
The microscopic interpretation of electron noise in Schottky barrier diodes
T.GONZALEZ, D.PARDO, L.VARANI, L.REGGIANI

Universal electrical characteristics and frequency limits of the permeable base transistor
P.CHENEVIER, G.KAMARINOS, G.PANANAKAKIS

Permeable base transistors with Schottky and junction gates
F.VAN RIJS, D.J.OOSTRA, J.M.L.van ROOIJ-MULDER, C.E.TIMMERING

Optimization of submicron microwave transistors by lateral scaling

Sub-20 ps ECL bipolar technology with high breakdown voltage
Y.KATSUMATA, N.ITOH, H.NAKAJIMA, K.INOU, T.IINUMA, S.MATSUDA, C.YOSHINO, Y.TSUBOI, H.IWAI

Physical Modelling of Dopant Diffusion: a Key Point for Deep Submicron CMOS Process Simulation (invited)
D.MATHIOT

Stress dependent oxidation simulations for submicron technologies
Z.KRIVOKAPIC, B.LIU

2D numerical simulation of titanium silicide growth
P.FORNARA, A.PONCET
Technical Contents

Va4
A model for fast oxide thickness and surface concentration extraction for tunnel oxide capacitors
L.HASPESLAGH, G.VANHOREBECK, L.DEFERM

155

Va5
High concentration boron diffusion study using a complete point defect and dynamic nucleation model
E.VANDENBOSSCHE, B.BACCUS

159

Va6
Two-dimensional modelling of silo isolation structures
D.COLLARD, V.SENEZ, B.BACCUS

163

Va7
Sensitivity of PNP doping profiles to annealing conditions - role of dynamic clustering phenomena -
B.BACCUS, E.VANDENBOSSCHE, A.MONROY, D.COLLARD, H.JAOUEN, M.ROCHE

167

Session Vb: CMOS Devices

Vb1
Technologies for System Integration: Constraints and Solutions in Modular Process Development (invited)
K.RODDE

173

Vb2
The design, fabrication and characterization of 0.15μm MOS devices
H.HANAFI, P.COANE, A.DALLY, T.LII, D.MASTIN

181

Vb3
Silicon based MIS devices with organic molecular monolayer as ultra-thin insulating film
D.VUILLAUME, P.FONTAINE, J.COLLET, D.DERESMES, M.GARET, F.RONDELEZ

185

Vb4
Identification of thermal and electrical time constants in SOI MOSFETs from small signal measurements
B.M.TENBROEK, W.REDMAN-WHITE, M.J.UREN, M.S.L.LEE, M.C.L.WARD

189
Vb5
Physical properties of silicon CMOS devices operated between liquid helium and room temperature
K.RAIS, I.M.HAFEZ, A.EMRANI, F.BALESTRA, G.GHIBAUDO, M.HAOND

193

Vb6
Process and design considerations for latch-up optimization on deep sub-micron CMOS technology
C.LEROUX, G.GUEGAN, M.LERME

197

Session Vc: Si Bipolar Devices

Vc1
Selective Epitaxial Bipolar Technology for 25 to 40Gb/s ICs (invited)
T.F.MEISTER, R.STENGL, A.FELDER, H.M.REIN

203

Vc2
Physical identification of an excess base current component in silicided half-micrometer polysilicon-emitter bipolar transistors
A.CHANTRE, J.KIRTSCH, N.DEGORS

211

Vc3
Optimization of BF2 implanted $pnp$ polysilicon emitter bipolar transistors using rapid thermal annealing
N.E.MOISEIWITSCH, P.ASHBURN

215

Vc4
$P$ mono-/p polysilicon layer: separation of influences on electron transport and their processing dependences
B.HU, H.H.BERGER

219

Vc5
ABCMOS3: a high precision, high speed, modular BiCMOS process for analog/digital applications

223

Vc6
High current properties of combined Schottky/pn diodes; interaction between closely located Schottky and pn diodes
J.OLSSON, H.NORDE, B.EDHOLM

227
Session VIA: Plenary Invited Papers

VIa1
The new limits of optical lithography
W.H.ARNOLD

VIa2
Design Aspects for Multilayer Interconnections on ICs
H.SCHETTLER

Session VIIa: CMOS Technology

VIIa1
The Future of High Density Packaging (invited)
B.C.JOHNSON

VIIa2
Framed poly buffer LOCOS technology for 0.35μm CMOS
V.M.H.MEYSSEN, A.H.MONTREE

VIIa3
A 0.25μm Fully Planarized CMOS Technology
M.ter BEEK, P.NUÑAN, S.CRANK, L.TA, R.BOOTH, K.V.ENKATARAMAN

VIIa4
Optimised drain/source engineering for 0.35μm NMOS transistors
J.L.OGIER, M.HAOND

VIIa5
Optimisation of a self-aligned twin well without channel stop implant for improved isolation of a 0.4μm CMOS process
S.DECOUTERE, G.VANCUYCK, L.DEFERM

Session VIIb: III-V Lasers

VIIb1
Strained Layer Quantum Well Lasers for Optical Communications (invited)
T.P.LEE, C.E.ZAH, R.BHAT
XXII Technical Contents

VIIib2
Investigation of the temperature dependence of threshold current density of GaInP/AlGaInP multi quantum well lasers
F.BARTH, B.KLEPSER, S.NAGEL, P.ERNST, M.MOSER, F.SCHOLZ, H.SCHWEIZER

VIIib3
Experimental analysis of laser diode thermal characteristics by voltage transient measurements
P.E.BAGNOLI, A.PICCIRILLO, S.MOTTET, M.THUAL, G.OLIVETI, M.CIAMPA

VIIib4
Carrier heating induced picosecond operation of GaInAsP/InP laser diode
V.I.TOLSTIKHIN, S.V.POLYAKOV

VIIib5
High power oscillation of reduced spatial hole burning DFB laser
A.TALNEAU, J.CHARIL, A.OUGAZZADEN, J.C.BOULEY, G.H.DUAN, F.GIRARDIN

Session VIIc: Si Ge Bipolar Devices

VIIc1
Si1-xGe x Heterojunction Bipolar Transistors: the future of silicon bipolar technology or not? (invited)
P.ASHBURN, Z.A.SHAFI, I.R.C.POST, H.J.GREGORY

VIIc2
Influence of the base/collector-heterojunction on the large and small signal behaviour of Si/SiGe-HBTs and consequences for applications in high-speed ICs
J.N.ALBERS, H.U.SCHREIBER, W.GEPPERT

VIIc3
Influence of the Ge fraction and distribution in the base of Si/SiGe-HBTs on the transit frequency
M.ROßBERG, F.SCHWIERZ, D.SCHIPANSKI, H.U.SCHREIBER, J.N.ALBERS
VIIc4
On the electron minority carrier mobility and the effective bandgap in heterojunction bipolar transistors with strained Si$_{1-x}$Ge$_x$-base

VIIc5
Reactive ion etching damage to strained Si$_{1-x}$Ge$_x$ heterojunction diodes
W. ZHONG, D. MISRA

Session VIIIa: Modelling of Silicon and Compound Semiconductor Devices

VIIIa1
Physical Modelling and Simulation of Advanced Si-Devices - An Industrial Approach (invited)

VIIIa2
Modelling of anomalous boron diffusion in Si/Si$_{1-x}$Ge$_x$ HBTs
H. J. GREGORY, M. MOUIS, D. MATHIOT, D. J. ROBBINS, J. GLASPER, P. ASHBURN, S. NIGRIN

VIIIa3
Current filamentation and thermal instability in a power BJT array cell
V. AXELRAD, J. G. ROLLINS, S. J. MOTZNY

VIIIa4
Transient analysis of CML and CMOS inverters using Monte-Carlo simulation
S. GALDIN, C. BRISSET, P. DOLLFUS, P. HESTO

VIIIa5
Use of electrothermal simulation to analyze thermal breakdown on N+/P/P+ diode during ESD pulse
C. BUJ, C. LEROUX, J. P. CHANTE

VIIIa6
Application of 2D-hydrodynamic energy modelling to the optimization of planar-doped pseudomorphic HEMTs
K. SHERIF, G. SALMER, O. L. EL-SAYED
VIIIa7
Low frequency noise and excess currents due to trap-assisted tunneling in double barrier resonant tunneling diodes 355
M.J.DEEN

Session VIIIb: CMOS Devices

VIIIb1
2D numerical investigation of gate structure, band alignment and delta-doping effects on the transconductance and cutoff frequency of submicron Si/SiGe FET's 361
S.P.VOINGESCU, P.RABKIN, C.A.T.SALAMA, P.A.BLAKEY

VIIIb2
p-MOSFETs and MODFETs with a strained Si$_{1-x}$Ge$_x$ channel layer 365
A.H.READER, S.COLAK, A.H.MONTREE, W.J.KERSTEN, D.J.GRAVESTEIJN

VIIIb3
Reduced hot electron degradation using delta-doped MOSFETs 369

VIIIb4
Dark Current characterization in CCD's 373
W.J.TOREN, J.BISSCHOP

VIIIb5
A high density multi-bit/analog DRAM cell 377
W.KIM, J.KIH, G.KIM, S.JUNG, G.AHN, K.H.OH

VIIIb6
Optimization of a submicron HIMOS flash $E^2$PROM cell for implementation in a virtual ground array configuration 381
J.VAN HOUTDT, D.WELLEKENS, L.HASPESLAGH, L.DEFERM, G.GROESENEKEN, H.E.MAES

VIIIb7
Temperature cross-over effect of carrier avalanche induced by band-to-band tunneling in ULSI devices 385
M.ORLOWSKI, S.W.SUN, D.BURNETT
Session VIIIc: Dielectrics

VIIIc1
Field Isolation for the Gigabit Era Devices (invited)
S.DELEONIBUS

VIIIc2
0.25μm CMOS with N₂O nitrided gate oxides
H.G.POMP, H.LIFKA, G.PAULZEN, A.H.MONTREE, P.H.WOERLEE, R.WOLTJER

VIIIc3
Thermal oxidation of lightly- and heavily-doped silicon in pure N₂O
S.C.SUN', H.Y.CHANG

VIIIc4
Comparison of RTP N₂O- and NH₃-nitrided thin SiO₂ films
D.BOUVET, N.NOVKOVSKI, J.MI, P.LETOURNEAU, M.DUTOIT, F.PIO, C.RIVA, N.BELLAFOIRE

VIIIc5
A new optimized process for low pressure nitridation of thin thermal gate oxide
V.THIRION, K.BARLA, A.STRABONI

VIIIc6
Reduction of bulk oxide trapping in poly-Si gated MOS capacitors by fluorination
V.V.AFANAS'EV, J.M.M.de NIJS, P.BALK

Session IXa: Characterisation

IXa1
Hot carrier monitoring in NMOS transistors by visible light emission
I.SCHÖNSTEIN, J.MÜLLER, U.HILLERINGMANN, K.GOSER

IXa2
Pulsed drain current: a highly sensitive technique for interface characterization in VLSI MOSFET's
H.HADDARA
XXVI Technical Contents

IXa3
Simultaneous measurement of carrier mobility and recombination lifetime on a testchip in MOS-technology by means of the Shockley-Haynes-experiment within the temperature range 98K to 398K
B.KRÜGER, Th.FRIESE, A.SCHMIDT, H.G.WAGEMANN

IXa4
A compact method for measuring parasitic resistances in bipolar transistors
G.VERZELLESI, A.CHANTRE, R.TURETTA, M.CAPPELLIN, P.PAVAN, E.ZANONI

IXa5
Impact Ionization Effect in Complementary CHarge Injection Transistor
C.TEDESCO, M.MASTRAPASQUA, C.CANALI, S.LURYI, E.ZANONI

Session IXb: III-V HeteroFETs

IXb1
InP channel HFETs with high breakdown voltage and low channel noise
K.NAIT-ZERRAD, G.POST, F.BALESTRA

IXb2
DC characterization and low-frequency noise in δ-, pulse- and uniformly-doped GaAs/AlGaAs MODFETs
Z.M.SHI, M.A.PY, H.J.BÜHLMANN, M.ILEGEMS

IXb3
Current transient spectroscopy on AlInAs/GaAlInAs heterojunction field effect transistors
S.ABABOU, F.DUCROQUET, G.GUILLOT, Ph.BERTHIER, L.GIRAUDET, J.P.FRASEUTH

IXb4
DC characterization of Ga0.51In0.49P/GaAs insulated-gate inverted-structure HEMT grown by Gas source molecular beam epitaxy (GSMBE)
S.S.LU, C.L.HUANG
A piezo-electric field effect transistor (PEFET) using Al$_{0.35}$Ga$_{0.65}$As/In$_{0.2}$Ga$_{0.8}$As/GaAs strained layer structure on (111)B GaAs substrate

C.L. HUANG, S.S. LU

Numerical investigation of leakage current of Schottky contacts on InAlAs/InGaAs/InP heterostructures

P. ELLRODT, W. BROCKERHOFF, C. HEEDT, F. J. TEGUDE

Pd/Ge based ohmic contacts to InGaAs/InAlAs High Electron Mobility Transistors

J. TARDY, P. CREMILLIEU, J. L. LECLERCQ, P. ROJO-ROMEO, J. F. ROCHETTE

Relationship between the 200-mm wafer size and the submicron technologies (invited)

M. BRILLOUËT

Comparison of Ti and Ni Salicides as regards the electrical conductance of silicided films

T. OHGURO, T. MORIMOTO, A. NISHIYAMA, Y. USHIKU, H. IWAI

Selective CVD TiSi$_2$ for Sub-0.5μm N+P/+ CMOS devices

M. HAOND, J. L. REGOLINI

High resolution delineation of bi-dimensional dopant profiles in silicon: early stages of diffusion from cobalt silicide layers

F. LA VIA, C. SPINELLA, E. RIMINI

Electrophysical parameters of the SiO$_2$-Si system in very high temperatures

B. MAJKUSIAK, R. B. BECK
IXc6
Electrical properties of thin oxides for MOSFETs in the Poly-
Si/SiO₂/6H silicon carbide system
C.M.ZETTERLING, M.ÖSTLING

Session Xa: Late News Session

Not included in the Proceedings

Session XIa: Plenary Invited Papers

XIa1
STORM: A European Platform for Sub-Micron Technology
Simulation and Optimisation
S.K.JONES, C.LOMBARDI, A.PONCET, C.HILL, H.JAOUEN, J.LORENZ,
C.LYDEN, K.de MEYER, J.PELKA, M.RUDAN, S.SOLMI

XIa2
CMOS Device Architecture and Technology for the 0.25
Micron to 0.025 Micron Generations
H.IWAI

Session XIIa: Characterisation

XIIa1
Characterization of semiconductor device structures with
ultrathin layers by Raman scattering
A.MINTAIROV, K.SMEKALIN

XIIa2
Charge pumping at cryogenic temperatures
C.R.ViŚWANATHAN, J.T.HSU, R.DIVAKARUNI, X.LI

XIIa3
Cryogenic on-chip high frequency device characterization
P.CROZAT, D.BOUCHON, J.C.HENÄUX, F.ANIEL, R.ADDE, G.VERNET

XIIa4
Observation and modelling of the gate-source capacitance
overshoot in polysilicon TFTs
S.W.B.TAM, P.MIGLIORATO, M.J.IZZARD, C.REITA
Technical Contents

XIIa5
Two dimensional profiling of doped layers by spreading resistance measurements and atomic force microscopy on chemical etched surfaces
V.PRIVITERA, V.RAINERI, W.VANDERVORST, T.CLARYSSE, L.HELLEMANS, J.SNAUWAERT

XIIa6
A comprehensive analysis of the relaxation phenomena in MOSFET's after uniform Fowler-Nordheim injection
C.PAPADAS, N.REVIL, G.Ghibaudo, P.MORTINI, G.PANANAKAKIS

Session XIIb: CMOS Technology

XIIb1
The ADEQUAT project for development and transfer of 0.25μm logic CMOS modules (invited)

XIIb2
Chemical mechanical polishing for planarisation of advanced IC processes
H.LIFKA, W.DOEDEL, T.SOUTS, P.H.WOERLEE

XIIb3
The effect on overlay of wafer distortion induced by dielectric reflow process
G.RIVERA, C.CLEMENTI

XIIb4
Raman spectroscopy measurement of local stress induced by LOCOS and trench structures in the silicon substrate
I.DE WOLF, H.E.MAES, K.YALLUP

XIIb5
Double polysilicon capacitors in 1μm analogue CMOS technology
P.K.HURLEY, L.WALL, A.MATHEWSON
Session XIIc: EPROM

XIIc1
Status, Trends, Comparison and Evolution of EPROM and FLASH EEPROM Technologies (invited)  
A.BERGEMONT  
575

XIIc2
Effect of polysilicon doping and oxidation conditions on tunnel oxide performance for EEPROM devices  
P.O'SULLIVAN, F.NAUGHTON, H.T.BENZ, G.FERNHOLZ, S.HAESELER, A.MATHEWSON  
583

XIIc3
Analysis of the fabrication process of multilayer vertical stacked capacitors  
E.STRASSER, S.SELBERHERR  
587

XIIc4
A new very high density full feature EEPROM cell with minimum process complexity  
A.BERGEMONT, H.HAGGAG, M.HART, L.ANDERSON  
591

XIIc5
Charge trapping/detrapping in Si$_3$N$_4$/SiO$_2$ stacked dielectric layer deposited by LPCVD with in situ HF vapor cleaning  
P.MAZOYER, F.MONDON, F.MARTIN, B.GUILLAUMOT, J.HARTMANN  
595

Session XIIIa: CMOS Modelling

XIIIa1
The Numerical Simulation of Non-Volatile-Memories (invited)  
C.LOMBARDI, S.KEENEY, R.BEZ, L.RAVAZZI, D.CANTARELLI, F.PICCININI, A.CONCANNON, A.MATHEWSON  
601

XIIIa2
Simulation of non-equilibrium transport in deep submicron MOSFETs  
P.H.BRICOUT, E.DUBOIS, R.FAUQUEMBERGUE  
609

XIIIa3
Performance in RF power MOSFET's device for GSM radiotelephony  
K.KASSMI, F.OMS, P.ROSSEL, H.TRANDUC  
613
XIIIa4  
A physically based DC- and AC-model for vertical smart power DMOS transistors  
M.STIFTINGER, W.SOPPA, S.SELBERHERR  

XIIIa5  
Weak inversion models for nMOS gate-all-around (GAA) devices  
P.FRANCIS, A.TERAO, D.FLANDRE, F.Van De WIELE  

XIIIa6  
The influence of technological parameters on ultra-short gate Si-NMOS transistor performances  
M.CHAREF, F.DESSENNE, J.L.THOBEL, L.BAUDRY, R.FAUQUEMBERGUE  

XIIIa7  
Physical modeling of nanoelectronic devices  
E.ABRAMCZYK, J.D.MEINDL  

Session XIIIb: III-V HBT and Sensors  

XIIIb1  
Issues in the Design of Heterojunction Bipolar Transistors for Large Signal Analogue and High Efficiency Microwave Power (invited)  
A.J.HOLDEN  

XIIIb2  
Safe operating current density and failure modes of carbon doped base AlGaAs/GaAs HBTs  
S.J.PRASAD, E.HULTINE  

XIIIb3  
A new GaAlAs-GaInP-GaAs HBT technology for digital and microwave applications  
P.LAUNAY, P.DESROUSSEAUX, J.DANGLA, V.FOURNIER, J.L.BENCHIMOL, F.ALEXANDRE, A.M.DUCHENOIS, M.MENOUNI  

XIIIb4  
Rapid, on-line extraction of base resistance of HBTs and correlation with minimum noise figure  
S.J.PRASAD, J.LASKAR
Highly sensitive gated InGaAs/InP Hall sensors with low temperature coefficient of the sensitivity
R.KYBURZ, J.SCHMID, R.S.POPOVIC, H.MELCHIOR

Physics of AlGaAs/InGaAs/GaAs heterostructures for high performance magnetic sensors
V.MOSSER, S.CONTRERAS, S.ABOULHOUDA, Ph.LORENZINI, F.KOBBI, J.L.ROBERT, K.ZEKENTES

SAW transduction technique for GaAs microelectronics compatible acoustoelectronic devices
R.MISKINIS, P.RUTKOWSKI

SOI Technology Outlook for Sub 0.25μm CMOS, Challenges and Opportunities (invited)
B.DAVARI, G.G.SHAHIDI

Analysis of carrier transport and heating in ultra-small SOI n-MOSFETs
C.FIEGNA, H.IWAI, E.SANGIORGI, B.RICCO

A 6 device SOI new technology for mixed analog-digital and rad-hard applications
J.P.BLANC, J.BONAIME, E.DELEVOYE, J.de PONTCHARRA, J.GAUTIER, F.MARTIN, R.TRUCHE

High frequency bipolar transistor on SIMOX
U.MAGNUSSON, H.NORSTRÖM, W.KAPLAN, S.ZHANG, M.JARGELIUS, D.SIGURD

High temperature gate capacitances of thin-film SOI MOSFETs
B.GENTINNE, D.FLANDRE, J.P.COLINGE, F.Van De WIELE
XIIIc6
Evaluation of CMOS/SOI devices on Plasma-thinned bonded silicon wafers
M.MATLOUBIAN, J.PINTER, K.AUBUCHON, O.MARSH, B.McCLAIN, D.P.MATHUR, T.FENG, G.GARDOPEE

XIIIc7
Self-heating effects on static and dynamic SOI operation
D.YACHOU, J.GAUTIER, C.RAYNAUD

Session XIVa: Plenary Invited Papers

XIVa1
BiCMOS: Status and Future Trends
M.ROCHE

XIVa2
Overview on Active Matrix Display Technology
G.H.van LEEUWEN, R.A.HARTMAN

Session XVa: Reliability and Testing

XVa1
Reliability modelling with respect to circuit applications
(invited)
J.F.VERWEIJ, A.J.MOUTHAAAN

XVa2
Noise figure degradation under emitter-base reverse stress for high-frequency bipolar ICs
N.ITOH, Y.KATSUMATA, H.IWAI

XVa3
A new intrinsic charge loss analysis on 16 Mb EPROM
F.MONDON, P.MAZOYER, B.GUILLAUMOT

XVa4
Electrical performances of a mounted chip in a plastic package
F.NDAGIJIMANA, B.CABON, J.CHILO
XXXIV Technical Contents

XVa5
Diffusion-induced degradation of AlGaAs/GaAs heterojunction bipolar transistors by thermal stress 739
S.HONG, J.KIM, C.PARK, J.LEE, T.WON

Session XVb: III-V Quantum and Hetero Devices

XVb1
Novel Quantum Effect Devices for Future Functional Logic Gates (invited) 745
T.MIZUTANI

XVb2
Performance of 0.2 μm planar doped pseudomorphic and lattice matched HEMTs on GaAs and InP 753
Y.BAEYENS, T.SKRABKA, M.Van HOVE, W.De RAEDT, B.NAUWELAERS, M.Van ROSSUM

XVb3
Physical behaviour of pseudomorphic HEMTs at low temperatures 757
F.ANIEL, P.CROZAT, A.De LUSTRA, R.ADDE, M.Van HOVE, W.De RAEDT, M.Van ROSSUM, Y.JIN

XVb4
Broad transconductance plateau region and high current GaAs/InGaAs pseudomorphic HEMT's utilizing a graded InxGa1-xAs channel 761
W.C.HSU, H.M.SHIEH, Y.H.WU, R.T.HSU

XVb5
Characterization of InAlAs/InGaAs HFETs with high indium content in the channel grown on GaAs substrate 765
N.RORSMAN, C.KARLSSON, H.ZIRATH, S.WANG, T.ANDERSSON

Session XVc: Micromachining, Microsystems

XVc1
Twin-channel (P and N) CCD image sensor with cross anti-blooming 771
E.ROKS, L.ESSE, L.SANKARANARAYANAN, W.HUININK
XVc2
Cross sensitivity elimination in a 3-dimensional magnetic sensor
B.WANG, D.MISRA

XVc3
Study of a new SiO₂ etching process allowing deep and anisotropic trenches. Optimization of new reactor parameters by means of actinometry
L.MORGENROTH, L.PECCOUD, P.BAUSSAND

XVc4
Silicon bulk machining of electrostatic micromotors fabrication and potential applications
H.ZIAD, A.BOUNHİR, S.SPIRKOVITCH, F.BAILLIEU, T.BOUROUINA, J.MARTY, S.RIGO, A.L'HOIR

XVc5
Model of detection for a modulated conductivity sensor: application for a NOₓ gas sensor
J.GUTIERREZ, L.ARES, J.I.ROBLA, I.SAYAGO, M.C.HORRILLO, J.A.AGAPITO

XVc6
Channel waveguides through silicon wafers for optically coupled 3D integrated circuits
V.I.RUDAKOV, V.V.POSTERNAK

Session XVIa: Reliability and Testing

XVIa1
Physical Mechanisms of Hot-Carrier-Induced Degradation in Deep-Submicron MOSFETs (invited)
S.CRISTOLOVEANU

XVIa2
Design and Characterisation of the Well module for a 6 transistor CMOS SRAM cell in a 0.5μm lithography CMOS technology
C.LE MOUELLIC, O.LE NEEL, K.RÖDDE

XVIa3
Reliability of 0.35μm devices: impact of ultra-shallow LDD-source/drains
M.ORLOWSKI, C.MAZURE, C.GUNDERSON
The gate-to-drain overlap effects on the hot-carrier induced degradation of LDD P-channel MOSFET's

Y.PAN

813

Effects of drain engineering on 0.35 \( \mu \)m NMOS hot-carrier degradation

G.PAULZEN, R.WOLTJER, A.H.MONTREE, J.POLITIEK

817

Radiation hardness of a bonded silicon-vacuum-silicon field effect structure with 0.1 MGy capability

R.HARRIS, G.ENSELL, A.BRUNNSCHWEILER

821

Detailed analysis of buried oxide degradation induced by hot-carrier injection

E.GUICHARD, S.CRISTOLOVEANU, G.REIMBOLD, G.BOREL

825

Comparative study of hot-carrier degradation in p+ and n+ poly p-MOSFET's of a 0.5\( \mu \)m CMOS technology

C.MONSERIE, R.BELLENS, G.GROESENEKEN, H.E.MAES

829

Gate voltage dependence of the hot-carrier degradation of large-angle-tilt implanted drain (LATID) and standard LDD N-MOSFET's

A.BRAVAIX, D.VUILLAUME

833

Microwave Optical Links: A New Generation of Optoelectronic Integrated Circuits (invited)

D.DECOSTER, J.C.RENAUD

839

Burst noise and tunneling currents in Lattice-Mismatched InP/InGaAs/InP photodetector arrays

D.POGANY, S.ABABOU, G.GUILLOT, B.VILOTITCH, C.LENOBLE

847
First demonstration of nanosecond photon timing in the near-infrared with InGaAs/InP detectors
C. SAMORI, A. LACAITA, P. A. FRANCHESE, S. COVA, P. WEBB

Structural optimization of quantum confined Stark shift in InGaAs/InGaAsP quantum wells
T. TÜTKEN, B. J. HAWDON, M. ZIMMERMANN, A. HANGLEITER, V. HÄRLE, F. SCHOLZ

Extrinsic GaAs: Mn detectors for 8 - 12 μm
V. RYABOKON, V. BESPALOV, A. EMELYANOV, N. SAMSONOV

Linewidth and mode structure of proton-implanted vertical cavity laser diodes
B. MÖLLER, R. MICHALZIK, E. ZEEB, T. HACKBARTH, K. J. EBELING

Output characteristics of surface emitting laser diodes with short external cavity
T. WIPIEJEWSKI, K. PANZLAFF, E. ZEEB, K. J. EBELING

A novel surface emitting GaAs/AlGaAs laser diode beam steering device based on surface mode emission
A. KÖCK, C. GMACHL, M. ROSENBERGER, E. GORNIK, C. THANNER, L. KORTE

High power vertical cavity laser diodes
E. ZEEB, T. HACKBARTH, K. J. EBELING

An intelligent 600V vertical IGBT on SIMOX substrate
B. MÜTTERLEIN, F. VOGT, J. WEYERS, H. VOGT

A novel MCT structure for power integrated circuits
Q. HUANG, G. A. J. AMARATUNGA
XXVIII Technical Contents

XVIc3
Optimisation of high voltage (1200V) MOS transistor: voltage handling capabilities and switching behaviour
G.CHARITAT, F.OMS, B.BEYDOUN, N.NOLHIER, P.ROSSEL, A.PEYRE-LAVIGNE

XVIc4
Investigation of a novel wiring scheme for 700-1000-V HVIC's
A.F.J.MURRAY, W.A.LANE

XVIc5
On P-I-N diode parameters and static properties at elevated temperatures and high current densities-experiment vs simulation
H.BLEICHER, M.ROSLING, P.JONSSON, F.MASSZI, F.VOJDAH, M.ISBERG, E.NORDLANDER

XVIc6
Overvoltage protection with a CMOS-compatible BJT
G.SCHROM, S.SELBERHERR, F.UNTERLEITNER, J.TRONTELJ, V.KUNC

XVIc7
A new Lateral NPN transistor structure for power MOSFETs with on-chip protection
R.ZAMBRANO, G.MONTALBANO, S.LEONARDI

Session XVIIc: Late News Session
Not included in the proceedings

LVIC (Low Voltage-Low Power ICs) Symposium

General Introduction, Motivation and Requirements for LV-LP IC's
J.BOREL

Opportunities for Scaling FET's for Gigascale Integration (GSI)
B.AGRAWAL, V.K.DE, J.D.MEINDL

Design of Low-Voltage Low-Power IC's
E.VITTOZ
Technical Contents

Technology and device design constraints for low voltage-low power sub-0.1μm CMOS devices
M.KOYANAGI 935

Performance, Reliability and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable
D.FOTY, E.J.NOWAK 943

Low Voltage and Low Power issues and applications
R.H.SALTERS 949

"PACT" - A Programmable Analog CMOS Transmission Circuit for Electronic Telephone Sets