Circuit and System Approaches for the Design of Low-Voltage, Low-Power Delta-Sigma Modulators

Vom Fachbereich 18
Elektrotechnik und Informationstechnik
der Technischen Universität Darmstadt
zur Erlangung der Würde eines
Doktor-Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

von

Dipl.-Ing. M.Sc.
Massoud Momeni
geboren am 2. Dezember 1981
in Dubai, Vereinigte Arabische Emirate

Referent: Prof. Dr. Dr. h. c. mult. Manfred Glesner
         Technische Universität Darmstadt

Korreferent: Prof. Dr.-Ing. Maurits Ortmanns
             Universität Ulm

Tag der Einreichung: 27.04.2010
Tag der mündlichen Prüfung: 28.06.2010

D17
Darmstädter Dissertationen
# Table of Contents

1 Introduction and Overview ........................................... 1
   1.1 Motivation ..................................................... 1
   1.2 Research Scope and Objectives .............................. 3
   1.3 Thesis Outline ................................................ 4

2 Fundamentals of ΔΣ A/D Conversion ............................... 7
   2.1 Nyquist-Rate A/D Conversion ................................ 8
       2.1.1 Sampling .................................................. 8
       2.1.2 Quantization and Additive White Noise Approximation ... 10
       2.1.3 In-Band Quantization Error Power and Dynamic Range ... 13
   2.2 Oversampling and Noise-Shaping A/D Converters ............ 14
       2.2.1 Oversampling .............................................. 14
       2.2.2 Noise Shaping ............................................ 16
       2.2.3 Basic ΔΣ ADC Architecture ............................. 19
           2.2.3.1 Anti-Aliasing Filter ......................... 20
           2.2.3.2 ΔΣ Modulator .................................. 20
           2.2.3.3 Decimator ........................................ 20
       2.2.4 Signal and Noise Transfer Function and 1st-Order ΔΣ Modulation .... 22
       2.2.5 Performance Metrics ................................. 25
       2.2.6 Ideal ΔΣ Modulator Performance ....................... 27
           2.2.6.1 Dynamic Range as a Function of the Modulator Order ... 28
           2.2.6.2 Dynamic Range as a Function of the Oversampling Ratio ... 28
           2.2.6.3 Dynamic Range as a Function of the Quantizer Resolution ... 29
       2.2.7 Single-Stage ΔΣ Architectures ......................... 31
           2.2.7.1 First-Order ΔΣ Modulator ........................ 31
           2.2.7.2 Second-Order ΔΣ Modulator ........................ 33
           2.2.7.3 Higher-Order ΔΣ Modulators ..................... 35
       2.2.8 Cascade ΔΣ Architectures ............................... 37
           2.2.8.1 Third-Order Cascade ΔΣ Modulator ............ 39
2.2.8.2 L-0 Cascade ΔΣ Modulator ...................... 41
2.2.9 Multi-Bit ΔΣ Architectures ......................... 43
  2.2.9.1 Internal Multi-Bit ADC and DAC Architecture .... 45
  2.2.9.2 Element Trimming ................................ 46
  2.2.9.3 Dual Quantization ................................ 47
  2.2.9.4 Dynamic Element Matching ....................... 47
  2.2.9.5 Digital Correction of DAC Nonlinearity .......... 48
2.3 Summary ................................................. 48

3 State of the Art in Low-Voltage Circuit Design and ΔΣ A/D Conversion 51
  3.1 History .................................................. 52
  3.2 Low-Voltage Circuit Design and ΔΣ A/D Conversion .......... 56
    3.2.1 Dynamic Amplifiers ................................ 59
    3.2.2 Inverter-Based Switched-Capacitor Circuitry ........ 61
    3.2.3 Sturdy-MASH ΔΣ Modulation ....................... 62
    3.2.4 Digital Correction ................................. 63
    3.2.5 Switched-Opamps ................................... 64
    3.2.6 Reset-Opamps ...................................... 65
    3.2.7 Switched-RC ....................................... 66
  3.3 Survey of Published ΔΣ A/D Converters .................. 67
    3.3.1 Figure of Merit ................................... 67
    3.3.2 Survey ............................................ 68
  3.4 Summary ................................................. 76

4 Comparator-Based Switched-Capacitor Circuits 79
  4.1 Basic Principle ........................................ 80
    4.1.1 Input Sampling ..................................... 80
    4.1.2 Traditional Opamp-Based Switched-Capacitor Gain Stage ..... 80
    4.1.3 Comparator-Based Switched-Capacitor Gain Stage ........ 81
  4.2 Practical CBSC Gain Stage .............................. 83
    4.2.1 Preset Phase ...................................... 84
    4.2.2 Coarse Charge Transfer Phase ....................... 84
    4.2.3 Fine Charge Transfer Phase ........................ 87
  4.3 Linearity Performance .................................. 88
    4.3.1 Offset due to Finite Comparator Delay .............. 89
    4.3.2 Offset due to Finite Switch On-Resistance .......... 91
    4.3.3 Total Offset ...................................... 92
    4.3.4 Nonlinearity due to Finite Comparator Delay ....... 93
### Table of Contents

4.3.5 Nonlinearity due to Finite Switch On-Resistance ........................................ 97
4.3.6 Total Nonlinearity ......................................................................................... 99
4.3.7 Total Single-Ramp Charge Transfer Time ...................................................... 100
4.3.8 Total Dual-Ramp Charge Transfer Time ......................................................... 102

4.4 Advanced CBSC Circuit Techniques ................................................................. 110
4.4.1 Overshoot Correction .................................................................................... 110
4.4.1.1 Limitation due to the Summing Node Voltage ........................................... 111
4.4.1.2 Limitation due to the Output Voltage Swing ............................................. 114
4.4.2 Multiple-Ramp Charge Transfer .................................................................... 115
4.4.3 Comparison of Single-, Dual-, and Multiple-Ramp Charge Transfers .......... 122

4.5 Benefits and Drawbacks of the CBSC Technique .............................................. 127
4.6 Summary .......................................................................................................... 128

5 ΔΣ Modulator Hardware Implementation ............................................................. 131
5.1 A 1.2-V 2nd-Order Lowpass ΔΣ Modulator in 0.13-μm CMOS ....................... 132
  5.1.1 Modulator Topology ...................................................................................... 132
  5.1.2 Fully-Differential CBSC stage ...................................................................... 133
  5.1.3 Switched-Capacitor Realization .................................................................. 135
  5.1.4 Capacitor Sizing .......................................................................................... 135
  5.1.5 Switches ...................................................................................................... 136
  5.1.6 Miller Amplifier .......................................................................................... 138
    5.1.6.1 Finite DC Gain ...................................................................................... 139
    5.1.6.2 Settling and Frequency Response .......................................................... 139
    5.1.6.3 Common-Mode Feedback ..................................................................... 140
  5.1.7 Folded Cascode Amplifier .......................................................................... 141
  5.1.8 Comparator .................................................................................................. 143
  5.1.9 CBSC Logic .................................................................................................. 144
  5.1.10 Current Sources ....................................................................................... 145
  5.1.11 Quantizer .................................................................................................. 145
  5.1.12 Clock Generator ....................................................................................... 146
  5.1.13 Performance .............................................................................................. 148

5.2 A Class of 1.2-V Lowpass Single- and Multi-Stage ΔΣ Modulators in 0.13-μm CMOS ........................................................................................................... 153
  5.2.1 Modulator Topologies .................................................................................. 153
  5.2.2 Differential CBSC Stage ............................................................................. 155
  5.2.3 Switched-Capacitor Realization ................................................................. 156
  5.2.4 Operational Amplifier ................................................................................ 160
  5.2.5 Comparator ................................................................................................ 164
TABLE OF CONTENTS

5.2.6  Quantizer ............................................. 165
5.2.7  Performance .......................................... 165
5.3    Summary ............................................ 169

6  Experimental Prototyping and Test Results 171
6.1    Chip Floorplan, Layout, and Pin-Out Description .................. 172
6.2    Printed Circuit Boards, Test Equipment and Setup .................. 174
6.3    Test Results and Performance Comparison with the State of the Art 179
6.4    Summary ............................................ 182

7  Conclusions and Future Work 183
7.1    Contributions of the Work ................................ 184
7.2    Directions for Future Work ................................ 186

A  Overview of Published ΔΣ A/D Converters 189

B  Impact of Circuit Nonidealities on the Implementation of Switched-Capacitor Resonators 203
B.1   Lowpass and Bandpass ΔΣ Modulators .......................... 203
B.2   Switched-Capacitor Integrators ................................ 205
      B.2.1  Finite Opamp Gain $A$ .................................. 206
      B.2.2  Nonzero Input Capacitance $C_n$ .......................... 207
      B.2.3  Finite Unity-Gain Bandwidth $f_u$ ....................... 207
B.3   Integrator-Based Switched-Capacitor Resonators .................. 208
      B.3.1  Impact of Integrator-Related Circuit Nonidealities ........ 209
B.4   Switched-Capacitor Delay Cells ................................ 210
      B.4.1  Finite Opamp Gain $A$ .................................. 210
      B.4.2  Nonzero Input Capacitance $C_n$ .......................... 211
      B.4.3  Finite Unity-Gain Bandwidth $f_u$ ....................... 211
B.5   Delay-Based Switched-Capacitor Resonators ....................... 211
      B.5.1  Impact of Delay-Cell-Related Circuit Nonidealities ........ 213
B.6   Simulation Results and Discussion ................................ 215
B.7   Summary ............................................ 215

References 239