CONTENTS

Chapter 1  Number Systems, Number Representations, and Codes 1

1.1 Number Systems 1
  1.1.1 Binary Number System 4
  1.1.2 Octal Number System 7
  1.1.3 Decimal Number System 9
  1.1.4 Hexadecimal Number System 10
  1.1.5 Arithmetic Operations 12
  1.1.6 Conversion Between Radices 22

1.2 Number Representations 29
  1.2.1 Sign Magnitude 29
  1.2.2 Diminished-Radix Complement 31
  1.2.3 Radix Complement 34
  1.2.4 Arithmetic Operations 38

1.3 Binary Codes 59
  1.3.1 Binary Weighted and Nonweighted Codes 59
  1.3.2 Binary-to-BCD Conversion 63
  1.3.3 BCD-to-Binary Conversion 64
  1.3.4 Gray Code 65

1.4 Error Detection and Correction Codes 68
  1.4.1 Parity 68
  1.4.2 Hamming Code 70
  1.4.3 Cyclic Redundancy Check Code 72
  1.4.4 Checksum 73
  1.4.5 Two-Out-Of-Five Code 75
  1.4.6 Horizontal and Vertical Parity Check 75

1.5 Serial Data Transmission 77

1.6 Problems 78

Chapter 2  Minimization of Switching Functions 83

2.1 Boolean Algebra 83
2.2 Algebraic Minimization 92
2.3 Karnaugh Maps 95
  2.3.1 Map-Entered Variables 113
2.4 Quine-McCluskey Algorithm 118
  2.4.1 Petrick Algorithm 123

2.5 Problems 128
Chapter 3  Combinational Logic 137

3.1 Logic Primitive Gates 138
  3.1.1 Wired-AND and Wired-OR Operations 148
  3.1.2 Three-State Logic 150
  3.1.3 Functionally Complete Gates 150

3.2 Logic Macro Functions 154
  3.2.1 Multiplexers 155
  3.2.2 Decoders 173
  3.2.3 Encoders 185
  3.2.4 Comparators 189

3.3 Analysis of Combinational Logic 194

3.4 Synthesis of Combinational Logic 205

3.5 Problems 223

Chapter 4  Combinational Logic Design
Using Verilog HDL 231

4.1 Built-In Primitives 232

4.2 User-Defined Primitives 267
  4.2.1 Defining a User-Defined Primitive 267
  4.2.2 Combinational User-Defined Primitives 267

4.3 Dataflow Modeling 289
  4.3.1 Continuous Assignment 289
  4.3.2 Reduction Operators 312
  4.3.3 Conditional Operator 315
  4.3.4 Relational Operators 318
  4.3.5 Logical Operators 320
  4.3.6 Bitwise Operators 322
  4.3.7 Shift Operators 326

4.4 Behavioral Modeling 328
  4.4.1 Initial Statement 329
  4.4.2 Always Statement 332
  4.4.3 Intrastatement Delay 339
  4.4.4 Interstatement Delay 341
  4.4.5 Blocking Assignments 343
  4.4.6 Nonblocking Assignments 345
  4.4.7 Conditional Statement 351
  4.4.8 Case Statement 356
  4.4.9 Loop Statements 365
  4.4.10 Tasks 370
  4.4.11 Functions 374

4.5 Structural Modeling 378
  4.5.1 Module Instantiation 378
  4.5.2 Ports 379
Chapter 5  Computer Arithmetic 425

5.1 Fixed-Point Addition 426
  5.1.1 Ripple-Carry Addition 428
  5.1.2 Carry Lookahead Addition 429
5.2 Fixed-Point Subtraction 433
5.3 Fixed-Point Multiplication 436
  5.3.1 Sequential Add-Shift 439
  5.3.2 Booth Algorithm 442
  5.3.3 Bit-Pair Recoding 448
  5.3.4 Array Multiplier 453
5.4 Fixed-Point Division 456
  5.4.1 Restoring Division 458
  5.4.2 Nonrestoring Division 460
5.5 Decimal Addition 462
  5.5.1 Addition With Sum Correction 463
  5.5.2 Addition Using Multiplexers for Sum Correction 464
5.6 Decimal Subtraction 467
5.7 Decimal Multiplication 472
  5.7.1 Multiplication Using Read-Only Memory 472
5.8 Decimal Division 477
  5.8.1 Division Using Table Lookup 477
5.9 Floating-Point Arithmetic 477
  5.9.1 Floating-Point Addition/Subtraction 482
  5.9.2 Floating-Point Multiplication 489
  5.9.3 Floating-Point Division 493
  5.9.4 Rounding Methods 495
5.10 Problems 497

Chapter 6  Computer Arithmetic Design
Using Verilog HDL 503

6.1 Fixed-Point Addition 503
  6.1.1 High-Speed Full Adder 504
  6.1.2 Four-Bit Ripple Adder 509
  6.1.3 Carry Lookahead Adder 515
6.2 Fixed-Point Subtraction 520
6.3 Fixed-Point Multiplication 527
  6.3.1 Booth Algorithm 527
  6.3.2 Array Multiplier 532
6.4 Decimal Addition 538
   6.4.1 BCD Addition With Sum Correction 539
   6.4.2 BCD Addition Using Multiplexers for Sum Correction 543
6.5 Decimal Subtraction 549
6.6 Problems 560

Chapter 7  Sequential Logic 565

  7.1 Analysis of Synchronous Sequential Machines 566
    7.1.1 Machine Alphabets 566
    7.1.2 Storage Elements 569
    7.1.3 Classes of Sequential Machines 573
    7.1.4 Methods of Analysis 582
    7.1.5 Analysis Examples 591
  7.2 Synthesis of Synchronous Sequential Machines 605
    7.2.1 Synthesis Procedure 606
    7.2.2 Synchronous Registers 619
    7.2.3 Synchronous Counters 623
    7.2.4 Moore Machines 634
    7.2.5 Mealy Machines 641
    7.2.6 Output Glitches 648
  7.3 Analysis of Asynchronous Sequential Machines 655
    7.3.1 Fundamental-Mode Model 656
    7.3.2 Methods of Analysis 658
    7.3.3 Hazards 663
    7.3.4 Oscillations 674
    7.3.5 Races 676
  7.4 Synthesis of Asynchronous Sequential Machines 679
    7.4.1 Synthesis Procedure 679
    7.4.2 Synthesis Examples 681
  7.5 Analysis of Pulse-Mode Asynchronous Sequential Machines 706
    7.5.1 Analysis Procedure 708
  7.6 Synthesis of Pulse-Mode Asynchronous Sequential Machines 715
    7.6.1 Synthesis Procedure 715
  7.7 Problems 722

Chapter 8  Sequential Logic Design Using Verilog HDL 739

  8.1 Synchronous Sequential Machines 740
  8.2 Asynchronous Sequential Machines 770
  8.3 Pulse-Mode Asynchronous Sequential Machines 790
  8.4 Problems 808
Chapter 9  Programmable Logic Devices 821

9.1 Programmable Read-Only Memory 822
  9.1.1 Combinational Logic 823
  9.1.2 Sequential Logic 827
9.2 Programmable Array Logic 831
  9.2.1 Combinational Logic 833
  9.2.2 Sequential Logic 834
9.3 Programmable Logic Arrays 845
  9.3.1 Combinational Logic 845
  9.3.2 Sequential Logic 847
9.4 Field-Programmable Gate Arrays 854
9.5 Problems 862

Chapter 10  Digital and Analog Conversion 869

10.1 Operational Amplifier 869
10.2 Digital-to-Analog Conversion 872
  10.2.1 Binary-Weighted Resistor Network Digital-to-Analog Converter 873
  10.2.2 R – 2R Resistor Network Digital-to-Analog Converter 878
10.3 Analog-to-Digital Conversion 883
  10.3.1 Comparators 883
  10.3.2 Counter Analog-to-Digital Converter 885
  10.3.3 Successive Approximation Analog-to-Digital Converter 886
  10.3.4 Simultaneous Analog-to-Digital Converter 890
10.4 Problems 894

Chapter 11  Magnetic Recording Fundamentals 899

11.1 Return to Zero 900
11.2 Nonreturn to Zero 901
11.3 Nonreturn to Zero Inverted 902
11.4 Frequency Modulation 903
11.5 Phase Encoding 905
11.6 Modified Frequency Modulation 906
11.7 Run-Length Limited 906
11.8 Group-Coded Recording 908
11.9 Peak Shift 911
11.10 Write Precompensation 912
11.11 Vertical Recording 914
11.12 Problems 915