Test and Diagnosis of Analogue, Mixed-signal and RF Integrated Circuits

The system on chip approach

Edited by Yichuang Sun

The Institution of Engineering and Technology
Contents

Preface xv
List of contributors xix

1 Fault diagnosis of linear and non-linear analogue circuits 1
Yichuang Sun

1.1 Introduction 1
1.2 Multiple-fault diagnosis of linear circuits 3
  1.2.1 Fault incremental circuit 3
  1.2.2 Branch-fault diagnosis 4
  1.2.3 Testability analysis and design for testability 6
  1.2.4 Bilinear function and multiple excitation method 8
  1.2.5 Node-fault diagnosis 9
  1.2.6 Parameter identification after k-node fault location 10
  1.2.7 Cutset-fault diagnosis 12
  1.2.8 Tolerance effects and treatment 15
1.3 Class-fault diagnosis of analogue circuits 15
  1.3.1 Class-fault diagnosis and general algebraic method for classification 16
  1.3.2 Class-fault diagnosis and topological technique for classification 18
  1.3.3 t-class-fault diagnosis and topological method for classification 19
1.4 Fault diagnosis of non-linear circuits 21
  1.4.1 Fault modelling and fault incremental circuits 21
  1.4.2 Fault location and identification 24
  1.4.3 Alternative fault incremental circuits and fault diagnosis 26
1.5 Recent advances in fault diagnosis of analogue circuits 29
  1.5.1 Test node selection and test signal generation 29
Test and diagnosis of analogue, mixed-signal and RF integrated circuits

1.5.2 Symbolic approach for fault diagnosis of analogue circuits
1.5.3 Neural-network- and wavelet-based methods for analogue fault diagnosis
1.5.4 Hierarchical approach for large-scale circuit fault diagnosis

1.6 Summary
1.7 References

2 Symbolic function approaches for analogue fault diagnosis
Stefano Manetti and Maria Cristina Piccirilli

2.1 Introduction
2.2 Symbolic analysis
  2.2.1 Symbolic analysis techniques
  2.2.2 The SAPWIN program
2.3 Testability and ambiguity groups
  2.3.1 Algorithms for testability evaluation
  2.3.2 Ambiguity groups
  2.3.3 Singular-value decomposition approach
  2.3.4 Testability analysis of non-linear circuits
2.4 Fault diagnosis of linear analogue circuits
  2.4.1 Techniques based on bilinear decomposition of fault equations
  2.4.2 Newton–Raphson-based approach
  2.4.3 Selection of the test frequencies
2.5 Fault diagnosis of non-linear circuits
  2.5.1 PWL models
  2.5.2 Transient analysis models for reactive components
  2.5.3 The Katznelson-type algorithm
  2.5.4 Circuit fault diagnosis application
  2.5.5 The SAPDEC program
2.6 Conclusions
2.7 References

3 Neural-network-based approaches for analogue circuit fault diagnosis
Yichuang Sun and Yigang He

3.1 Introduction
3.2 Fault diagnosis of analogue circuits with tolerances using artificial neural networks
  3.2.1 Artificial neural networks
  3.2.2 Fault diagnosis of analogue circuits
  3.2.3 Fault diagnosis using ANNs
4 Hierarchical/decomposition techniques for large-scale analogue diagnosis

Peter Shepherd

4.1 Introduction 113
4.1.1 Diagnosis definitions 114
4.2 Background to analogue fault diagnosis 115
4.2.1 Simulation before test 115
4.2.2 Simulation after test 116
4.3 Hierarchical techniques 121
4.3.1 Simulation after test 121
4.3.2 Simulation before test 131
4.3.3 Mixed SBT/SAT approaches 135
4.4 Conclusions 137
4.5 References 138

5 DFT and BIST techniques for analogue and mixed-signal test

Mona Safi-Harb and Gordon Roberts

5.1 Introduction 141
5.2 Background 142
5.3 Signal generation 146
5.3.1 Direct digital frequency synthesis 146
5.3.2 Oscillator-based approaches 147
5.3.3 Memory-based signal generation 148
5.3.4 Multi-tones 149
5.3.5 Area overhead 150
5.4 Signal capture 151
5.5 Timing measurements and jitter analysers 154
  5.5.1 Single counter 154
  5.5.2 Analogue-based interpolation techniques:
      time-to-voltage converter 155
  5.5.3 Digital phase-interpolation techniques: delay line 156
  5.5.4 Vernier delay line 157
  5.5.5 Component-invariant VDL for jitter measurement 159
  5.5.6 Analogue-based jitter measurement device 160
  5.5.7 Time amplification 162
  5.5.8 PLL and DLL – injection methods for PLL tests 163
5.6 Calibration techniques for TMU and TDC 164
5.7 Complete on-chip test core: proposed architecture in Reference 11 and
   its versatile applications 166
  5.7.1 Attractive and flexible architecture 166
  5.7.2 Oscilloscope/curve tracing 168
  5.7.3 Coherent sampling 169
  5.7.4 Time domain reflectometry/transmission 169
  5.7.5 Crosstalk 169
  5.7.6 Supply/substrate noise 170
  5.7.7 RF testing – amplifier resonance 171
  5.7.8 Limitations of the proposed architecture in Reference 11 172
5.8 Recent trends 172
5.9 Conclusions 173
5.10 References 174

6 Design-for-testability of analogue filters 179
Yichuang Sun and Masood-ul Hasan

6.1 Introduction 179
6.2 DfT by bypassing 181
  6.2.1 Bypassing by bandwidth broadening 181
  6.2.2 Bypassing using duplicated/switched opamp 186
6.3 DfT by multiplexing 188
  6.3.1 Tow-Thomas biquad filter 188
  6.3.2 The Kerwin–Huelsman–Newcomb biquad filter 189
  6.3.3 Second-order OTA-C filter 190
6.4 OBT of analogue filters 192
  6.4.1 Test transformations of active-RC filters 193
  6.4.2 OBT of OTA-C filters 196
  6.4.3 OBT of SC biquadratic filter 199
6.5 Testing of high-order analogue filters 201
6.5.1 Testing of high-order filters using bypassing 202
6.5.2 Testing of high-order cascade filters using multiplexing 203
6.5.3 Test of MLF OTA-C filters using multiplexing 205
6.5.4 OBT structures for high-order OTA-C filters 207
6.6 Summary 210
6.7 References 210

7 Test of A/D converters: From converter characteristics to built-in self-test proposals 213
Andreas Lechner and Andrew Richardson

7.1 Introduction 213
7.2 A/D conversion 214
7.2.1 Static A/D converter performance parameters 216
7.2.2 Dynamic A/D converter performance parameters 218
7.3 A/D converter test approaches 220
7.3.1 Set-up for A/D converter test 220
7.3.2 Capturing the test response 221
7.3.3 Static performance parameter test 222
7.3.4 Dynamic performance parameter test 226
7.4 A/D converter built-in self-test 228
7.5 Summary and conclusions 231
7.6 References 232

8 Test of \( \Sigma \Delta \) converters 235
Gildas Leger and Adoración Rueda

8.1 Introduction 235
8.2 An overview of \( \Sigma \Delta \) modulation: opening the ADC black box 236
8.2.1 Principle of operation: \( \Sigma \Delta \) modulation and noise shaping 236
8.2.2 Digital filtering and decimation 238
8.2.3 \( \Sigma \Delta \) modulator architecture 239
8.3 Characterization of \( \Sigma \Delta \) converters 243
8.3.1 Consequences of \( \Sigma \Delta \) modulation for ADC characterization 243
8.3.2 Static performance 244
8.3.3 Dynamic performance 246
8.3.4 Applying a FFT with success 248
8.4 Test of \( \Sigma \Delta \) converters 254
8.4.1 Limitations of the functional approach 255
8.4.2 The built-in self-test approach 255
8.5 Model-based testing 259
8.5.1 Model-based test concepts 259
8.5.2 Polynomial model-based BIST 262
8.5.3 Behavioural model-based BIST 264
8.6 Conclusions 271
8.7 References 273

9 Phase-locked loop test methodologies: Current characterization and production test practices 277
Martin John Burbidge and Andrew Richardson
9.1 Introduction: Phase-locked loop operation and test motivations 277
  9.1.1 PLL key elements’ operation and test issues 277
  9.1.2 Typical CP-PLL test specifications 282
9.2 Traditional test techniques 287
  9.2.1 Characterization focused tests 287
  9.2.2 Production test focused 298
9.3 BIST techniques 301
9.4 Summary and conclusions 306
9.5 References 306

10 On-chip testing techniques for RF wireless transceiver systems and components 309
Alberto Valdes-Garcia, Jose Silva-Martinez,
Edgar Sanchez-Sinencio
10.1 Introduction 309
10.2 Frequency-response test system for analogue baseband circuits 311
  10.2.1 Principle of operation 311
  10.2.2 Testing methodology 313
  10.2.3 Implementation as a complete on-chip test system with a digital interface 314
  10.2.4 Experimental evaluation of the FRCS 319
10.3 CMOS amplitude detector for on-chip testing of RF circuits 324
  10.3.1 Gain and 1-dB compression point measurement with amplitude detectors 327
  10.3.2 CMOS RF amplitude detector design 328
  10.3.3 Experimental results 330
10.4 Architecture for on-chip testing of wireless transceivers 333
  10.4.1 Switched loop-back architecture 333
  10.4.2 Overall testing strategy 337
  10.4.3 Simulation results 339
10.5 Summary and outlook 342
10.6 References 343
11 Tuning and calibration of analogue, mixed-signal and RF circuits 347
James Moritz and Yichuang Sun

11.1 Introduction 347
11.2 On-chip filter tuning 348
  11.2.1 Tuning system requirements for on-chip filters 348
  11.2.2 Frequency tuning and \( Q \) tuning 349
  11.2.3 Online and offline tuning 352
  11.2.4 Master–slave tuning 354
  11.2.5 Frequency tuning methods 355
  11.2.6 \( Q \) tuning techniques 359
  11.2.7 Tuning of high-order leapfrog filters 360
11.3 Self-calibration techniques for PLL frequency synthesizers 365
  11.3.1 Need for calibration in PLL synthesizers 365
  11.3.2 PLL synthesizer with calibrated VCO 366
  11.3.3 Automatic PLL calibration 368
  11.3.4 Other PLL synthesizer calibration applications 370
11.4 On-chip antenna impedance matching 371
  11.4.1 Requirement for on-chip antenna impedance matching 371
  11.4.2 Matching network 373
  11.4.3 Impedance sensors 376
  11.4.4 Tuning algorithms 377
11.5 Conclusions 378
11.6 References 378

Index 383