DSP INTEGRATED CIRCUITS

Lars Wanhammar
Linköping University

ACADEMIC PRESS
San Diego  London  Boston  New York  Sydney  Tokyo  Toronto
CONTENTS

1 DSP Integrated Circuits  1
  1.1 Introduction  1
  1.2 Digital Signal Processing  2
  1.3 Standard Digital Signal Processors  2
  1.4 Application-Specific ICs for DSP  4
    1.4.1 ASIC Digital Signal Processors  5
    1.4.2 Direct Mapping Techniques  6
  1.5 DSP Systems  7
    1.5.1 Facets  7
  1.6 DSP System Design  10
    1.6.1 Specification And Design Problem Capture  11
    1.6.2 Partitioning Techniques  12
    1.6.3 Design Transformations  17
    1.6.4 Complexity Issues  18
    1.6.5 The Divide-And-Conquer Approach  20
    1.6.6 VHDL  21
  1.7 Integrated Circuit Design  25
    1.7.1 System Design Methodology  26
    1.7.2 Technical Feasibility  26
    1.7.3 System Partitioning  27

2 VLSI Circuit Technologies  31
  2.1 Introduction  31
  2.2 MOS Transistors  31
    2.2.1 A Simple Transistor Model  33
  2.3 MOS Logic  36
    2.3.1 nMOS Logic  37
    2.3.2 CMOS Logic Circuits  39
    2.3.3 Propagation Delay in CMOS Circuits  40
    2.3.4 Power Dissipation in CMOS Circuits  44
    2.3.5 Precharge-Evaluation Logic  45
    2.3.6 Process Variations  46
    2.3.7 Temperature and Voltage Effects  46
2.4 VLSI Process Technologies 48
2.4.1 Bulk CMOS Technology 48
2.4.2 Silicon-on-Insulation (SOI) Technology 49
2.4.3 Bipolar Technologies—TTL 50
2.4.4 Bipolar Technologies—ECL 50
2.4.5 Bipolar–CMOS Technologies—BiCMOS 51
2.4.6 GaAs-Based Technologies 52

2.5 Trends in CMOS Technologies 53

3 Digital Signal Processing 59

3.1 Introduction 59
3.2 Digital Signal Processing 60
  3.2.1 Sensitivity 60
  3.2.2 Robustness 61
  3.2.3 Integrated Circuits 61

3.3 Signals 61
3.4 The Fourier Transform 62
3.5 The z-Transform 64
3.6 Sampling of Analog Signals 65
3.7 Selection of Sample Frequency 67

3.8 Signal Processing Systems 69
  3.8.1 Linear Systems 70
  3.8.2 SI (Shift-Invariant) Systems 70
  3.8.3 LSI (Linear Shift-Invariant) Systems 70
  3.8.4 Causal Systems 71
  3.8.5 Stable LSI Systems 72

3.9 Difference Equations 72

3.10 Frequency Response 73
  3.10.1 Magnitude Function 74
  3.10.2 Attenuation Function 75
  3.10.3 Phase Function 76
  3.10.4 Group Delay Function 77

3.11 Transfer Function 78

3.12 Signal-Flow Graphs 79

3.13 Filter Structures 80

3.14 Adaptive DSP Algorithms 82
  3.14.1 LMS (Least Mean Square) Filters 83
  3.14.2 RLS (Recursive Least Square) Lattice Filters 85

3.15 DFT—The Discrete Fourier Transform 86

3.16 FFT—The Fast Fourier Transform Algorithm 87
  3.16.1 CT-FFT—The Cooley–Tukey FFT 88
  3.16.2 ST-FFT (The Sande–Tukey FFT) 93
3.16.3 Winograd’s Fast Algorithm 96
3.16.4 IFFT (The Inverse FFT) 96

3.17 FFT Processor—Case Study 1 96
3.17.1 Specification 97
3.17.2 System Design Phase 97

3.18 Image Coding 98

3.19 Discrete Cosine Transforms 99
3.19.1 EDCT (Even Discrete Cosine Transform) 99
3.19.2 ODCT (Odd Discrete Cosine Transform) 101
3.19.3 SDCT (Symmetric Discrete Cosine Transform) 101
3.19.4 MSDCT (Modified Symmetric Discrete Cosine Transform) 102
3.19.5 Fast Discrete Cosine Transforms 104

3.20 DCT Processor—Case Study 2 105
3.20.1 Specification 107
3.20.2 System Design Phase 107

4 Digital Filters 115

4.1 Introduction 115

4.2 FIR Filters 115
4.2.1 Linear-Phase FIR Filters 116
4.2.2 Design of Linear-Phase FIR Filters 117
4.2.3 Half-Band FIR Filters 120
4.2.4 Complementary FIR Filters 122

4.3 Fir Filter Structures 122
4.3.1 Direct Form 122
4.3.2 Transposed Direct Form 123
4.3.3 Linear-Phase Structure 124
4.3.4 Complementary FIR Structures 125
4.3.5 Miscellaneous FIR Structures 126

4.4 FIR Chips 126

4.5 IIR Filters 127

4.6 Specification of IIR Filters 128
4.6.1 Analog Filter Approximations 129

4.7 Direct Design in the z-Plane 130

4.8 Mapping of Analog Transfer Functions 130
4.8.1 Filter Order 131

4.9 Mapping of Analog Filter Structures 137

4.10 Wave Digital Filters 138

4.11 Reference Filters 138

4.12 Wave Descriptions 140

4.13 Transmission Lines 141

4.14 Transmission Line Filters 143
4.15 Wave-Flow Building Blocks 144
  4.15.1 Circuit Elements 145
  4.15.2 Interconnection Networks 146
4.16 Design of Wave Digital Filters 150
  4.16.1 Feldtkeller's Equation 151
  4.16.2 Sensitivity 153
4.17 Ladder Wave Digital Filters 153
4.18 Lattice Wave Digital Filters 154
4.19 Bireciprocal Lattice Wave Digital Filters 162
4.20 Multirate Systems 166
4.21 Interpolation With an Integer Factor $L$ 166
  4.21.1 Interpolation Using FIR Filters 169
  4.21.2 Interpolation Using Wave Digital Filters 172
4.22 Decimation With A Factor $M$ 174
  4.22.1 HSP43220™ 175
4.23 Sampling Rate Change With a Ratio $L/M$ 176
4.24 Multirate Filters 177
4.25 Interpolator—Case Study 3 177

5 Finite Word Length Effects 187
5.1 Introduction 187
5.2 Parasitic Oscillations 188
  5.2.1 Zero-Input Oscillations 189
  5.2.2 Overflow Oscillations 191
  5.2.3 Periodic Input Oscillations 193
  5.2.4 Nonobservable Oscillations 193
  5.2.5 Parasitic Oscillations In Algorithms Using Floating-Point Arithmetic 194
5.3 Quantization In WDFs 195
5.4 Scaling of Signal Levels 198
  5.4.1 Safe Scaling 199
  5.4.2 FFT Scaling 201
  5.4.3 LP-Norms 201
  5.4.4 Scaling of Wide-Band Signals 203
  5.4.5 Scaling of Narrow Band Signals 206
5.5 Round-Off Noise 207
  5.5.1 FFT Round-Off Noise 210
  5.5.2 Error Spectrum Shaping 212
5.6 Measuring Round-Off Noise 213
5.7 Coefficient Sensitivity 215
  5.7.1 Coefficient Word Length 216
5.8 Sensitivity and Noise 216
5.9 Interpolator, Cont. 218  
5.10 FFT Processor, Cont. 218  
5.11 DCT Processor, Cont. 218  

6 DSP Algorithms 225  
6.1 Introduction 225  
6.2 DSP Systems 225  
6.2.1 DSP Algorithms 226  
6.2.2 Arithmetic Operations 228  
6.3 Precedence Graphs 229  
6.3.1 Parallelism in Algorithms 229  
6.3.2 Latency 230  
6.3.3 Sequentially Computable Algorithms 233  
6.3.4 Fully Specified Signal-Flow Graphs 234  
6.4 SFGs in Precedence Form 234  
6.5 Difference Equations 239  
6.6 Computation Graphs 243  
6.6.1 Critical Path 243  
6.6.2 Equalizing Delay 243  
6.6.3 Shimming Delay 244  
6.6.4 Maximum Sample Rate 245  
6.7 Equivalence Transformations 247  
6.7.1 Essentially Equivalent Networks 248  
6.7.2 Timing of Signal-Flow Graphs 249  
6.7.3 Minimizing the Amount of Shimming Delay 251  
6.7.4 Maximally Fast Critical Loops 251  
6.8 Interleaving and Pipelining 253  
6.8.1 Interleaving 254  
6.8.2 Pipelining 255  
6.8.3 Functional and Structural Pipelines 259  
6.8.4 Pipeline Interleaving 260  
6.9 Algorithm Transformations 261  
6.9.1 Block Processing 261  
6.9.2 Clustered Look-Ahead Pipelining 263  
6.9.3 Scattered Look-Ahead Pipelining 266  
6.9.4 Synthesis of Fast Filter Structures 267  

6.10 Interpolator, Cont. 267  

7 DSP System Design 277  
7.1 Introduction 277  
7.2 A Direct Mapping Technique 278
7.3 FFT Processor, Cont. 280
   7.3.1 First Design Iteration 281
   7.3.2 Second Design Iteration 283
   7.3.3 Third Design Iteration 290

7.4 Scheduling 292

7.5 Scheduling Formulations 293
   7.5.1 Single Interval Scheduling Formulation 294
   7.5.2 Block Scheduling Formulation 297
   7.5.3 Loop-Folding 297
   7.5.4 Cyclic Scheduling Formulation 298
   7.5.5 Overflow and Quantization 305
   7.5.6 Scheduling of Lattice Wave Digital Filters 310

7.6 Scheduling Algorithms 313
   7.6.1 ASAP and ALAP Scheduling 313
   7.6.2 Earliest Deadline and Slack Time Scheduling 314
   7.6.3 Linear Programming 315
   7.6.4 Critical Path List Scheduling 315
   7.6.5 Force-Directed Scheduling 315
   7.6.6 Cyclo-Static Scheduling 317
   7.6.7 Maximum Spanning Tree Method 320
   7.6.8 Simulated Annealing 321

7.7 FFT Processor, Cont. 323
   7.7.1 Scheduling of the Inner Loops 325
   7.7.2 Input and Output Processes 327

7.8 Resource Allocation 328
   7.8.1 Clique Partitioning 330

7.9 Resource Assignment 331
   7.9.1 The Left-Edge Algorithm 331

7.10 Interpolator, Cont. 334
   7.10.1 Processor Assignment 336
   7.10.2 Memory Assignment 336
   7.10.3 Memory Cell Assignment 338

7.11 FFT Processor, Cont. 341
   7.11.1 Memory Assignment 341
   7.11.2 Butterfly Processor Assignment 344
   7.11.3 Input and Output Process Assignment 347

7.12 DCT Processor, Cont. 348

8 DSP Architectures 357

8.1 Introduction 357

8.2 DSP System Architectures 357

8.3 Standard DSP Architectures 359
   8.3.1 Harvard Architecture 360
   8.3.2 TMS32010™ 360
8.3.3 TMS320C25™ and TMS320C50™ 361
8.3.4 TMS320C30™ 362
8.3.5 TMS320C40™ 363
8.3.6 Motorola DSP56001™ and DSP56002™ 363
8.3.7 Motorola DSP96001™ and DSP96002™ 364

8.4 Ideal DSP Architectures 365
8.4.1 Processing Elements 366
8.4.2 Storage Elements 367
8.4.3 Interconnection Networks 367
8.4.4 Control 367
8.4.5 Synchronous and Asynchronous Systems 368
8.4.6 Self-Timed Systems 368
8.4.7 Autonomous Bit-Serial PEs 369

8.5 Multiprocessors And Multicomputers 370

8.6 Message-Based Architectures 371
8.6.1 Interconnection Topologies 372

8.7 Systolic Arrays 374

8.8 Wave Front Arrays 376
8.8.1 Datawave™ 377

8.9 Shared-Memory Architectures 379
8.9.1 Memory Bandwidth Bottleneck 380
8.9.2 Reducing the Memory Cycle Time 380
8.9.3 Reducing Communications 381
8.9.4 Large Basic Operations 383

9 Synthesis of DSP Architectures 387

9.1 Introduction 387

9.2 Mapping of DSP Algorithms onto Hardware 388
9.2.1 Design Strategy 388

9.3 Uniprocessor Architectures 389

9.4 Isomorphic Mapping of SFGs 394
9.4.1 Cathedral I 395

9.5 Implementations Based on Complex PEs 397
9.5.1 Vector-Multiplier–Based Implementations 397
9.5.2 Numerically Equivalent Implementation 399
9.5.3 Numerically Equivalent Implementations of WDFs 402

9.6 Shared-Memory Architectures with Bit-Serial PEs 404
9.6.1 Minimizing the Cost 405
9.6.2 Uniform Memory Access Rate 405
9.6.3 Fast Bit-Serial Memories 407
9.6.4 Balancing the Architecture 407
9.6.5 Mode of Operation 408
9.6.6 Control 409
9.7 Building Large DSP Systems 410
9.8 Interpolator, Cont. 413
9.9 FFT Processor, Cont. 413
  9.9.1 Selecting the Interconnection Network 414
  9.9.2 Re-Partitioning the FFT 416
  9.9.3 The Final FFT Architecture 421
9.10 DCT Processor, Cont. 425
9.11 SIC (Single-Instruction Computer) 426
  9.11.1 Partitioning of Large DSP Systems 427
  9.11.2 Implementation of Various SIC Items 427

10 Digital Systems 437
  10.1 Introduction 437
  10.2 Combinational Networks 438
  10.3 Sequential Networks 439
  10.4 Storage Elements 440
    10.4.1 Static Storage Elements 441
    10.4.2 Dynamic Storage Elements 443
    10.4.3 Metastability 444
  10.5 Clocking of Synchronous Systems 444
    10.5.1 Single-Phase Clock 444
    10.5.2 Single-Phase Logic 445
    10.5.3 Two-Phase Clock 447
    10.5.4 Clock Skew 450
  10.6 Asynchronous Systems 450
  10.7 Finite State Machines (FSMs) 453
    10.7.1 Look-Ahead FSMs 453
    10.7.2 Concurrent Block Processing 456

11 Processing Elements 461
  11.1 Introduction 461
  11.2 Conventional Number Systems 461
    11.2.1 Signed-Magnitude Representation 462
    11.2.2 Complement Representation 463
    11.2.3 One's-Complement Representation 464
    11.2.4 Two's-Complement Representation 465
    11.2.5 Binary Offset Representation 467
  11.3 Redundant Number Systems 467
    11.3.1 Signed-Digit Code 468
    11.3.2 Canonic Signed Digit Code 469
    11.3.3 On-Line Arithmetic 470
  11.4 Residue Number Systems 470
11.5 Bit-Parallel Arithmetic 472
  11.5.1 Addition and Subtraction 472
  11.5.2 Bit-Parallel Multiplication 475
  11.5.3 Shift-and-Add Multiplication 476
  11.5.4 Booth’s Algorithm 477
  11.5.5 Tree-Based Multipliers 478
  11.5.6 Array Multipliers 479
  11.5.7 Look-Up Table Techniques 481
11.6 Bit-Serial Arithmetic 481
  11.6.1 Bit-Serial Addition and Subtraction 482
  11.6.2 Bit-Serial Multiplication 482
  11.6.3 Serial/Parallel Multiplier 482
  11.6.4 Transposed Serial/Parallel Multiplier 485
  11.6.5 S/P Multiplier-Accumulator 486
11.7 Bit-Serial Two-Port Adaptor 486
11.8 S/P Multipliers with Fixed Coefficients 489
  11.8.1 S/P Multipliers with CSDC Coefficients 490
11.9 Minimum Number of Basic Operations 491
  11.9.1 Multiplication with a Fixed Coefficient 492
  11.9.2 Multiple-Constant Multiplications 495
11.10 Bit-Serial Squarers 496
  11.10.1 Simple Squarer 496
  11.10.2 Improved Squarer 498
11.11 Serial/Serial Multipliers 500
11.12 Digit-Serial Arithmetic 502
11.13 The CORDIC Algorithm 502
11.14 Distributed Arithmetic 503
  11.14.1 Distributed Arithmetic 503
  11.14.2 Parallel Implementation of Distributed Arithmetic 507
11.15 The Basic Shift-Accumulator 507
11.16 Reducing the Memory Size 510
  11.16.1 Memory Partitioning 510
  11.16.2 Memory Coding 511
11.17 Complex Multipliers 512
11.18 Improved Shift-Accumulator 514
  11.18.1 Complex Multiplier Using Two-Phase Logic 515
  11.18.2 Complex Multiplier Using TSPC Logic 515
11.19 FFT Processor, Cont. 516
  11.19.1 Twiddle Factor PE 517
  11.19.2 Control PEs 520
  11.19.3 Address PEs 520
  11.19.4 Base Index Generator 521
  11.19.5 RAM Address PEs 522
11.20 DCT Processor, Cont. 522
12 Integrated Circuit Design  531

12.1 Introduction  531

12.2 Layout of VLSI Circuits  531
   12.2.1 Floor Planning and Placement  532
   12.2.2 Floor Plans  533
   12.2.3 Global Routing  534
   12.2.4 Detailed Routing  534
   12.2.5 Compaction by Zone Refining  536

12.3 Layout Styles  537
   12.3.1 The Standard-Cell Design Approach  537
   12.3.2 The Gate Array Design Approach  539
   12.3.3 The Sea-of-Gates Design Approach  541
   12.3.4 The Unconstrained-Cell Design Approach  541
   12.3.5 The Unconstrained Design Approach  544

12.4 FFT Processor, Cont.  545

12.5 DCT Processor, Cont.  547

12.6 Interpolator, Cont.  548

12.7 Economic Aspects  551
   12.7.1 Yield  551

Index  555