1 MOS Transistor Models

Introduction

1-1 MOSFET and Junction FET
   1-1-1 JFET
   1-1-2 MOST
   1-1-3 nMOST and pMOST

1-2 Capacitances and MOST Threshold Voltages
   1-2-1 MOS Capacitance
   1-2-2 Junction Capacitance
   1-2-3 MOST and JFET
   1-2-4 MOST Threshold Voltage
   1-2-5 Enhancement and Depletion MOST

1-3 MOST Linear Region and Saturation Region
   1-3-1 Large $v_{GS}$, Small $v_{DS}$, and Zero $v_{BS}$
   1-3-2 Large $v_{GS}$, Large $v_{DS}$, and Zero $v_{BS}$
   1-3-3 Large $v_{GS}$, Small $v_{DS}$, and Large $v_{BS}$

1-4 MOST Current-Voltage Characteristics
   1-4-1 Linear Region
   1-4-2 Linear Region: First-Order Model
   1-4-3 MOST in Saturation: First-Order Model
   1-4-4 Parameters $K'$ and $n$
   1-4-5 Plots of $i_{DS}$ versus $v_{GS}$ and $v_{BS}$
   1-4-6 Effective Channel Length and Width

1-5 Small-Signal Model in Saturation
   1-5-1 Transconductance $g_m$
2 Bipolar Transistor Models

2-1 Bipolar Transistor Operation
2-1-1 Structure
2-1-2 Depletion Layers
2-1-3 Base Doping
2-1-4 Forward Biasing
2-1-5 Base Transit Time

2-2 The Transistor Beta ($\beta$)
2-2-1 Beta Caused by Injection in the Emitter $\beta_{IE}$
2-2-2 Beta Caused by Recombination in the Base $\beta_{RB}$
2-2-3 Beta Caused by Recombination in the $EB$ Space Charge Layer
2-2-4 AC Beta $\beta_{AC}$

2-3 The Hybrid-$\pi$ Small-Signal Model
2-3-1 Transconductance $g_m$
2-3-2 Input Resistance $r_\pi$
2-3-3 Output Resistance $r_o$
2-3-4 Voltage Gain of Small-Signal Gain Stage
2-3-5 Junction Capacitances
2-3-6 Diffusion Capacitance $C_D$
2-3-7 Common-Emitter Configuration with Current Drive
2-3-8 Common-Emitter Configuration with Voltage Drive
2-3-9 Common-Collector and Common-Base Configurations

2-4 The Ohmic Resistances
2-4-1 The Base Resistance
2-4-2 Extrinsic Base Resistance
2-4-3 Intrinsic Base Resistance
2-4-4 The Collector Resistances
2-4-5 The Emitter Resistance

2-5 High-Injection and Other Second-Order Effects
2-5-1 High-Injection Effects in the Base
2-5-2 High-Injection Model of Beta
2-5-3 Base Resistance Effects
2-5-4 Graded Base
2-5-5 Collector Current Spreading
2-5-6 High-Injection Effects in the Collector
2-5-7 Bipolar Transistors for VLSI

2-6 Lateral $pnp$ Transistors
2-6-1 Substrate $pnp$ Transistors
2-6-2 Lateral \textit{pnp} Transistors 137
2-6-3 Base Width, Early Voltage, and Punchthrough 139
2-6-4 Base Resistance and Emitter Crowding 139
2-6-5 Applications with \textit{pnp}'s 139

2-7 Noise 142
2-7-1 Input Noise Sources 142
2-7-2 Equivalent Input Noise Sources 143
2-7-3 Noise Figure 144
2-7-4 Optimum $R_S$ 145
2-7-5 Optimum $NF$ 146
2-7-6 Optimum $I_C$ 146

2-8 Design Example 147
2-9 Other Components 147
2-9-1 Base Diffusion Resistors 147
2-9-2 Other Resistors 149
2-9-3 Temperature Coefficient 150
2-9-4 Voltage Coefficient 151
2-9-5 Frequency Dependence 151
2-9-6 Absolute and Relative Accuracy 152
2-9-7 Resistors in a CMOS Process 153
2-9-8 Thin Film Resistors 153
2-9-9 Capacitors 153
2-9-10 Inductors 155

2-10 Comparison between MOSTs and Bipolar Transistors 156
2-10-1 Input Current 157
2-10-2 DC Saturation Voltage 157
2-10-3 Transconductance-Current Ratio 159
2-10-4 Design Planning 160
2-10-5 Current Range 160
2-10-6 Maximum Frequency of Operation 160
2-10-7 Noise 161
Summary 162
Exercises 162
Appendix 2-1 164
References 169

3 Feedback and Sensitivity in Analog Integrated Circuits 170

Introduction 170
3-1 Feedback Theory 172
3-1-1 Basic Feedback Concepts and Definitions 177
3-1-2 Feedback Configurations and Classifications 185

3-2 Analysis of Feedback Amplifier Circuits 188
3-2-1 Analysis When the Feedback Network is One of the Four Basic Configurations in Fig. 3-7 189
3-2-2 Blackman's Impedance Relation 194
3-2-3 The Asymptotic Gain Relation 198

3-3 Stability Considerations in Linear Feedback Systems 200
3-3-1 Effect of Feedback on the System Natural Frequencies 202
3-3-2 The Use of Bode Plots in Stability Analysis 212
3-4  Sensitivity, Component Matching and Yield  
3-4-1  Component Matching  
3-4-2  Sensitivity Problem in Precision Analog Circuits  
3-4-3  Yield Considerations in Analog Integrated Circuits  
Summary  
Exercises  
Appendix 3-1: Approximate Calculations for a Two-Pole System when the Poles are Real and Widely Separated  
Appendix 3-2: Exact Calculation of the Bode Diagram for Two-Pole Systems  
References  

4  Elementary Transistor Stages  
Introduction  
4-1  MOST Single-Transistor Amplifying Stages  
4-1-1  Biasing  
4-1-2  Low Frequency Gain  
4-1-3  Bandwidth  
4-1-4  Full Circuit Performance at High Frequencies  
4-1-5  Unity-Gain Frequency and Gain-Bandwidth Product  
4-1-6  Noise Performance  
4-2  Bipolar Single-Transistor Amplifying Stages  
4-2-1  Biasing  
4-2-2  Gain for Voltage Drive and Current Drive  
4-2-3  Frequency Performance  
4-2-4  Gain-Bandwidth Product  
4-2-5  Input Impedance  
4-3  Source and Emitter Followers  
4-3-1  Source Followers  
4-3-2  Emitter Followers  
4-3-3  Noise Performance  
4-4  Cascade Transistors  
4-4-1  MOST Cascodes  
4-4-2  Bipolar Transistor Cascodes  
4-4-3  Noise Performance  
4-5  CMOS Inverter Stages  
4-5-1  DC Analysis of CMOS Inverters  
4-5-2  Low Frequency Gain  
4-5-3  Bandwidth  
4-5-4  Current Capability and Slew Rate  
4-5-5  Design Procedure  
4-5-6  Other MOST Inverters  
4-5-7  Bipolar Transistor Inverter Stages  
4-5-8  Noise Performance  
4-6  Cascade Stages  
4-6-1  Cascade Configurations  
4-6-2  Bandwidth of Cascade with Low $R_L$  
4-6-3  Cascade with Active Load  
4-6-4  Noise Performance  
4-6-5  High Voltage Cascade
6-2-1 Operating Principles and Biasing
6-2-2 Gain of the Miller OTA
6-2-3 Gain-Bandwidth Product and Phase-Margin
6-2-4 Design Plan
6-2-5 Miller BICMOS OTAs

6-3 Full Set of Characteristics of the Miller OTA
6-3-1 Full DC Analysis: Common-Mode Input Voltage Range
 versus Supply Voltage
6-3-2 Full DC Analysis: Output Range versus Supply Voltage
6-3-3 Full DC Analysis: Maximum Output Current (Source and Sink)
6-3-4 AC Analysis: Low Frequencies
6-3-5 Gain-Bandwidth versus Biasing Current
6-3-6 Slew Rate versus Load Capacitance
6-3-7 Output Voltage Range versus Frequency
6-3-8 Settling Time
6-3-9 Input Impedance
6-3-10 Output Impedance
6-3-11 Temperature Effects

6-4 Noise Analysis of OTAs
6-4-1 Noise Performance at Low Frequencies
6-4-2 Noise Performance at High Frequencies
6-4-3 Total Integrated Output Noise

6-5 Matching Specifications
6-5-1 Transistor Mismatch Model
6-5-2 Offset Voltage Definition
6-5-3 Mismatch Effects on a Current Mirror
6-5-4 Differential Stage with Active Load
6-5-5 Offset Drift
6-5-6 CMRR
6-5-7 Relation between Random $V_{osr}$ and $CMRR_r$
6-5-8 Relation between Systematic $V_{oss}$ and $CMRR_r$
6-5-9 CMRR versus Frequency
6-5-10 Offset and CMRR of the Miller CMOS OTA
6-5-11 Design for Low Offset and Drift
6-5-12 Offset in JFET Differential Amplifier
6-5-13 Offset and CMRR in Bipolar Differential Amplifier
6-5-14 Bias Current, Offset, and Drift

6-6 Power Supply Rejection Ratio
6-6-1 $PSRR_{DD}$ of Simple CMOS OTA
6-6-2 $PSRR_{SS}$ of Simple CMOS OTA
6-6-3 $PSRR_{DD}$ of the Miller CMOS OTA
6-6-4 $PSRR_{SS}$ of the Miller CMOS OTA

6-7 Design of Other OTAs
6-7-1 Symmetrical CMOS OTA
6-7-2 Cascode Symmetrical CMOS OTA
6-7-3 Symmetrical Miller CMOS OTA with High PSRR
6-7-4 Folded-Cascode CMOS OTA
6-7-5 Operational Current Amplifier (OCA)
6-8 Design Options
  6-8-1 Design for Optimum GBW or SR 595
  6-8-2 Compensation of Positive Zero 598
  6-8-3 Fully Differential or Balanced OTAs 601
6-9 Op Amp Examples 607
  6-9-1 CMOS op Amp Configurations 607
  6-9-2 Bipolar Op Amp Configurations 608
  6-9-3 BIMOS and BIFET Op Amp Configurations 610
Summary 612
Exercises 612
Appendix 6-1: Pole-Zero Doublets and Settling Time 622
Appendix 6-2: Amplifier Configurations 628
References 646

7 Fundamentals of Continuous-Time and Sampled-Data Active Filters 648
  Introduction 648
  7-1 Linear Filtering Concepts and Definitions 649
  7-2 Schemes for Integrated Analog Filters 652
    7-2-1 Active-RC and Active $G_m/C$ Filters 652
    7-2-2 Active-SC Filters 657
  7-3 Filter Types and Frequency Response Specifications 666
    7-3-1 Lowpass 668
    7-3-2 Highpass 670
    7-3-3 Bandpass 671
    7-3-4 Band-Reject 672
    7-3-5 Allpass or Delay Equalizer 672
    7-3-6 Basic Filter Specifications 675
  7-4 Determining a Nominal $H$ 678
    7-4-1 Maximally-Flat or Butterworth Filters 679
    7-4-2 Equi-Ripple (Chebyshev) Filters 681
    7-4-3 Cauer (Elliptic) Filters 684
    7-4-4 Bessel (Linear Phase) Filters 685
  7-5 Frequency Transforms 686
    7-5-1 $s$-to-$s$ Transforms 687
    7-5-2 $s$-to-$z$ Transforms 688
  7-6 Noise, DC Offset, Harmonic Distortion and Dynamic Range 690
  7-7 Sensitivity, Variability, and Yield 696
  7-8 Modeling and Analysis of Switched-Capacitor Filters 703
    7-8-1 Periodic Time-Variance in Biphase SC Filters 704
    7-8-2 $\phi^e$ and $\phi^o$ Decomposition 708
    7-8-3 Switched-Capacitor $z$-Domain Models 713
    7-8-4 Active SC Integrators 718
Summary 723
Exercises 724
Appendix 7-1: Sampled-Data Signals and Systems 732
References 756
# Design and Implementation of Integrated Active Filters

## Introduction

- Parasitic Capacitances in Integrated Filters
- Design of Practical Integrated Filter Components
  - Poly 1-Poly 2 Capacitor
  - MOST Analog Switch
  - Linearized MOST Resistor
  - Linearized OTA Transconductance
- Parasitics and Filter Precision
  - Reducing the Effect of Parasitics on Filter Precision
  - Parasitic Insensitive Switched-Capacitor Structures
- Automatic On-Chip Tuning
  - On-Chip Tuning Strategies
  - Frequency Tuning with PLL
  - $Q$ tuning with MLL
- PSRR, Clock Feedthrough and DC Offset
  - Clock Feedthrough and DC Offset Cancellation
  - Layout Measures to Improve PSRR
  - Balanced Active-RC and SC Design
- First-Order and Biquadratic Filter Stage Realizations
  - Realizing Real Poles and Zeros
  - Types of Biquads
- Fleischer-Laker Active-SC Biquads
  - Evaluation of the General Active-SC Biquad
  - Synthesis of Practical Active-SC Biquads
  - Examples
- Integrated Continuous-Time Fleischer-Laker Type Biquads
  - Active-RC Biquads using MOST-$R$’s
  - Active-$G_m/C$ Biquads using MOST-$G_m$’s
- High-Order Filter Implementation Using Cascaded Stages
  - Cascading First- and Second-Order Filter Stages
  - Time-Staggered Active-SC Stages
  - Settling Error Analysis of Delay Equalizers Realized as a Cascade of Active-SC AP Stages
- High-Order Filter Implementation Using Active Ladders
  - Sensitivity
  - Realization Using Signal Flow Graphs
  - Realizing All-Pole LP Filters
  - Realizing Symmetric All-Pole BP Filters
  - Realizing Finite Transmission Zeros
- Summary
- Exercises
- References

## Index

- Design and Implementation of Integrated Active Filters
- Parasitic Capacitances in Integrated Filters
- Design of Practical Integrated Filter Components
  - Poly 1-Poly 2 Capacitor
  - MOST Analog Switch
  - Linearized MOST Resistor
  - Linearized OTA Transconductance
- Parasitics and Filter Precision
  - Reducing the Effect of Parasitics on Filter Precision
  - Parasitic Insensitive Switched-Capacitor Structures
- Automatic On-Chip Tuning
  - On-Chip Tuning Strategies
  - Frequency Tuning with PLL
  - $Q$ tuning with MLL
- PSRR, Clock Feedthrough and DC Offset
  - Clock Feedthrough and DC Offset Cancellation
  - Layout Measures to Improve PSRR
  - Balanced Active-RC and SC Design
- First-Order and Biquadratic Filter Stage Realizations
  - Realizing Real Poles and Zeros
  - Types of Biquads
- Fleischer-Laker Active-SC Biquads
  - Evaluation of the General Active-SC Biquad
  - Synthesis of Practical Active-SC Biquads
  - Examples
- Integrated Continuous-Time Fleischer-Laker Type Biquads
  - Active-RC Biquads using MOST-$R$’s
  - Active-$G_m/C$ Biquads using MOST-$G_m$’s
- High-Order Filter Implementation Using Cascaded Stages
  - Cascading First- and Second-Order Filter Stages
  - Time-Staggered Active-SC Stages
  - Settling Error Analysis of Delay Equalizers Realized as a Cascade of Active-SC AP Stages
- High-Order Filter Implementation Using Active Ladders
  - Sensitivity
  - Realization Using Signal Flow Graphs
  - Realizing All-Pole LP Filters
  - Realizing Symmetric All-Pole BP Filters
  - Realizing Finite Transmission Zeros
- Summary
- Exercises
- References

- Index