VHDL
Analysis and Modeling of Digital Systems

Zainalabedin Navabi
Northeastern University

McGraw-Hill, Inc.
New York St. Louis San Francisco Auckland Bogotá Caracas
Lisbon London Madrid Mexico Milan Montreal
New Delhi Paris San Juan Singapore Sydney Tokyo Toronto
CONTENTS

Preface xvii

1 Hardware Design Environments 1
   1.1 Digital System Design Process 1
       1.1.1 Design Automation 3
   1.2 Hardware Description Languages 3
       1.2.1 A Language for Behavioral Descriptions 4
       1.2.2 A Language for Describing Flow of Data 5
       1.2.3 A Language for Describing Netlists 6
   1.3 Hardware Simulation 6
       1.3.1 Oblivious Simulation 8
       1.3.2 Event Driven Simulation 9
   1.4 Hardware Synthesis 10
   1.5 Levels of Abstraction 10
   1.6 Summary 13
       References 13
       Problems 14

2 VHDL Background 15
   2.1 VHDL Initiation 16
   2.2 Existing Languages 16
       2.2.1 AHPL 17
       2.2.2 CDL 17
       2.2.3 CONLAN 17
       2.2.4 IDL 17
       2.2.5 ISPS 17
       2.2.6 TEGAS 18
       2.2.7 TI-HDL 18
       2.2.8 ZEUS 18
   2.3 VHDL Requirements 18
       2.3.1 General Features 18
       2.3.2 Support for Design Hierarchy 19
       2.3.3 Library Support 19
2.3.4 Sequential Statement 20
2.3.5 Generic Design 21
2.3.6 Type Declaration and Usage 21
2.3.7 Use of Subprograms 21
2.3.8 Timing Control 22
2.3.9 Structural Specification 22
2.4 The VHDL Language 22
2.5 A VHDL Based Design Process 23
2.6 Summary 25
References 25
Problems 25

3 Basic Concepts in VHDL 26
3.1 Basic Concepts 26
3.1.1 An Illustrative Example 28
3.1.2 Interface Description 28
3.1.3 Architectural Description 30
3.1.4 Subprograms 35
3.1.5 VHDL Operators 37
3.2 Timing and Concurrency 37
3.2.1 Objects and Classes 39
3.2.2 Signals and Variables 40
3.2.3 Signal Assignments 40
3.2.4 Concurrent and Sequential Assignments 41
3.3 Conventions and Syntax 51
3.4 Summary 52
References 52
Problems 53

4 Structural Specification of Hardware 56
4.1 Parts Library 57
4.1.1 Inverter Model 57
4.1.2 NAND Gate Models 58
4.2 Wiring of Primitives 60
4.2.1 Logic Design of Comparator 60
4.2.2 VHDL Description of bit.comparator 62
4.3 Wiring Iterative Networks 67
4.3.1 Design of a Four Bit Comparator 67
4.3.2 VHDL Description of a Four Bit Comparator 69
4.4 Modeling a Test Bench 73
4.4.1 VHDL Description of A Simple Test Bench 74
4.4.2 Simulation 76
4.5 Binding Alternatives 77
4.6 Summary 82
References 82
Problems 83

5 Design Organization and Parameterization 87
5.1 Definition and Usage of Subprograms 88
5.1.1 A Functional Single Bit Comparator 88
5.1.2 Using Procedures in a Test Bench 90
5.1.3 Language Aspects of Subprograms 92
5.1.4 Utility Procedures 95

5.2 Packaging Parts and Utilities 96
5.2.1 Packaging Components 97
5.2.2 Packaging Subprograms 97

5.3 Design Parameterization 99
5.3.1 Using Default Values 103
5.3.2 Using Fixed Values 103
5.3.3 Passing Generic Parameters 104

5.4 Design Configuration 110
5.4.1 A General Purpose Test Bench 110
5.4.2 Configuring Nested Components 113
5.4.3 An Eight Bit Register Example 118

5.5 Design Libraries 124
5.6 Summary 128
References 128
Problems 128

6 Utilities for High Level Descriptions 131
6.1 Type Declarations and Usage 132
6.1.1 Enumeration Type for Multi-Value Logic 132
6.1.2 Using Real Numbers For Timing Calculations 135
6.1.3 Physical Types and RC Timing 137
6.1.4 Array Declarations 139
6.1.5 File Type and External File I/O 146

6.2 Subprogram Parameter Types and Overloading 149
6.3 Other Types and Type Related Issues 156
6.3.1 Subtypes 156
6.3.2 Record Types 157
6.3.3 Alias Declaration 158

6.4 Predefined Attributes 159
6.4.1 Array Attributes 160
6.4.2 Type Attributes 161
6.4.3 Signal Attributes 161

6.5 User-Defined Attributes 165
6.6 Packaging Basic Utilities 167

6.7 Summary 167
References 171
Problems 171

7 Dataflow Descriptions in VHDL 174
7.1 Multiplexing and Data Selection 174
7.1.1 General Multiplexing 176
7.1.2 Guarded Signal Assignments 180
7.1.3 Nesting Guarded Blocks 184
7.1.4 Resolving between Several Driving Values 186
7.1.5 MOS Implementation of Multiplexer 192
## Contents

7.1.6 A General Multiplexer 198

7.2 State Machine Description 200
7.2.1 A Sequence Detector 200
7.2.2 Allowing Multiple Active States 202
7.2.3 Outputs of Mealy and Moore Machines 204

7.3 Open Collector Gates 204

7.4 A General Dataflow Circuit 208

7.5 Updating Basic Utilities 212

7.6 Summary 212

References 214

Problems 215

8 Behavioral Description of Hardware 219

8.1 Process Statement 219
8.1.1 Declarative Part of a Process 220
8.1.2 Statement Part of a Process 220
8.1.3 Sensitivity List 222
8.1.4 A First Process Example 223
8.1.5 Syntactic Detail of Process Statements 225
8.1.6 Behavioral Flow Control Constructs 226

8.2 Assertion Statement 228
8.2.1 Sequential Use of Assertion Statements 228
8.2.2 Concurrent Assertion Statements 230

8.3 Sequential Wait Statements 231
8.3.1 A Behavioral State Machine 233
8.3.2 Two Phase Clocking 235
8.3.3 Implementing Handshaking 236

8.4 Formatted ASCII I/O Operations 240
8.4.1 Basic Screen Output 241
8.4.2 A Display Procedure 242
8.4.3 Simulation Report 243

8.5 MSI Based Design 247
8.5.1 Top Level Partitioning 247
8.5.2 Description of Components 248
8.5.3 Design Implementation 251

8.6 Summary 253

References 255

Problems 255

9 CPU Modeling and Design 259

9.1 Defining a Comprehensive Example 259

9.2 Parwan CPU 260
9.2.1 Memory Organization of Parwan 260
9.2.2 Instruction Set 260
9.2.3 Instruction Format 263
9.2.4 Programming in Parwan Assembly 266

9.3 Behavioral Description of Parwan 266
9.3.1 Timing and Clocking 267
9.3.2 Packages 267