
Phase-Locked Loops

Design, Simulation, and Applications

Roland E. Best

Sixth Edition



New York Chicago San Francisco Lisbon London Madrid
Mexico City Milan New Delhi San Juan Seoul
Singapore Sydney Toronto

Contents

Preface	xi
Chapter 1. Introduction to PLLs	1
1.1 Operating Principles of the PLL	1
1.2 Historical Background	5
1.3 Classification of PLL Types	6
Chapter 2. Mixed-Signal PLL Building Blocks	9
2.1 Block Diagram of the Mixed-Signal PLL	9
2.2 A Note on Phase Signals	10
2.3 Building Blocks of Mixed-Signal PLLs	12
2.4 Phase Detectors	13
2.4.1 Type 1: Multiplier phase detectors	13
2.4.2 Type 2: EXOR phase detectors	16
2.4.3 Type 3: JK-flipflop phase detectors	18
2.4.4 Type 4: Phase-frequency detectors (PFDs)	20
2.5 Loop Filters (First Order)	28
2.5.1 Type 1: Passive lead-lag filters	29
2.5.2 Type 2: Active lead-lag filters	30
2.5.3 Type 3: Active PI filters	31
2.6 Controlled Oscillators	32
2.6.1 Relaxation oscillators	32
2.6.2 Resonant oscillators	36
2.7 Down Scalers	36
Chapter 3. Mixed-Signal PLL Analysis	39
3.1 PLL Performance in the Locked State	39
3.2 The Mathematical Model for the Locked State	39
3.3 A Definition of Transfer Functions	41
3.3.1 The PLL transfer function for systems using the voltage output phase detector	41
3.3.2 The PLL transfer function for systems using current output phase detector	46
3.4 Transient Response of the PLL in the Locked State	47
3.4.1 Phase step applied to the reference input	47
3.4.2 Frequency step applied to the reference input	48
3.4.3 Frequency ramp applied to the reference input	49

3.5	Steady-State Error of the PLL	50
3.6	The Order of the PLL System	52
	3.6.1 The number of poles	52
	3.6.2 A special case: the first-order PLL	53
3.7	PLL Performance in the Unlocked State	53
3.8	Mathematical Model for the Unlocked State	53
3.9	Key Parameters of the PLL	62
	3.9.1 Hold range $\Delta\omega_H$	62
	3.9.2 Lock range $\Delta\omega_L$ and lock time T_L	65
	3.9.3 Pull-in range $\Delta\omega_P$ and pull-in time T_P	71
	3.9.4 Pull-out range $\Delta\omega_{PO}$	83
3.10	Optimizing the Lock Process	86
	3.10.1 Fastlock techniques	87
	3.10.2 Cycle slip reduction (CSR)	89
3.11	In-Lock detectors	91
Chapter 4. PLL Performance in the Presence of Noise		93
4.1	Sources and Types of Noise in a PLL	93
4.2	Defining Noise Parameters	95
4.3	The Impact of Noise on PLL Performance	96
4.4	Pull-in Techniques for Noisy Signals	104
	4.4.1 The sweep technique	104
	4.4.2 The switched-filter technique	106
Chapter 5. Design Procedure for Mixed-Signal PLLs		107
Chapter 6. Mixed-Signal PLL Applications Part 1: Integer-N Frequency Synthesizers		119
6.1	Synthesizers in Wireless and RF Applications	119
6.2	Integer- N Frequency Synthesizers without Prescalers	120
6.3	Integer- N Frequency Synthesizers with Prescalers	121
	6.3.1 Fixed division ratio prescalers	121
	6.3.2 Dual-modulus prescalers	122
	6.3.3 Four-modulus prescalers	124
6.4	Extending the Frequency Range with Mixers and Frequency Multipliers	126
6.5	Case Study: Designing an Integer- N PLL Frequency Synthesizer	128
6.6	Single-Loop and Multi-Loop Frequency Synthesizers	131
6.7	Phase Noise and Spurs in Integer Frequency Synthesizers	134
	6.7.1 Phase noise created by the reference oscillator	136
	6.7.2 Phase noise created by the VCO	145
	6.7.3 Spurs created by the phase detector	150
Chapter 7. Mixed-Signal PLL Applications Part 2: Fractional-N Frequency Synthesizers		159
7.1	Realization of Fractional Divider Ratios	159
7.2	Analog Spur Reduction Techniques	161
7.3	Digital Spur Reduction Techniques	165
7.4	Reviewing the $\Sigma\Delta$ Modulator	166
	7.4.1 The $\Sigma\Delta$ A/D converter	166
	7.4.2 The $\Sigma\Delta$ D/A converter	181
	7.4.3 The $\Sigma\Delta$ modulator used in frequency synthesizers	183
	7.4.4 Nonlinear effects in $\Sigma\Delta$ modulators	193

7.5	The Design Procedure for $\Sigma\Delta$ Modulators	194
7.6	Spurs, Fractional Spurs, and Subfractional Spurs	196
7.7	Alternative $\Sigma\Delta$ Modulators: The MASH Converter	197
Chapter 8. Mixed-Signal PLL Applications Part 3: Miscellaneous Applications		203
8.1	Retiming and Clock Signal Recovery	203
8.2	Motor-Speed Control	210
Chapter 9. Higher-Order Loops		217
9.1	Motivation for Higher-Order Loops	217
9.2	Analyzing the Stability of Higher-Order Loops	217
9.3	Designing Third-Order PLLs	220
9.3.1	The Passive lead-lag loop filter for voltage input	221
9.3.2	Passive lead-lag loop filter for current input	223
9.3.3	Active lead-lag loop filter	225
9.3.4	Active PI loop filter	227
9.4	Designing Fourth-Order PLLs	230
9.4.1	Passive lead-lag loop filters for voltage input	230
9.4.2	The passive lead-lag loop filter for current input	233
9.4.3	The active lead-lag loop filter	235
9.4.4	The active PI loop filter	238
9.5	Designing Fifth-Order PLLs	241
9.5.1	Passive lead-lag loop filter for voltage input	242
9.5.2	The passive lead-lag loop filter for current input	244
9.5.3	Active lead-lag loop filter	247
9.5.4	Active PI loop filter	251
9.6	The Key Parameters of Higher-Order PLLs	255
Chapter 10. Computer-Aided Design and Simulation of Mixed-Signal PLLs		257
10.1	Overview	257
10.2	Quick Tour	259
10.2.1	Configuring the PLL system	259
10.2.2	Designing the loop filter	260
10.2.3	Analyzing the stability of the loop	261
10.2.4	Getting the loop filter schematic	262
10.2.5	Running simulations	263
10.3	Simulations with and without Averaging	264
10.4	Simulations with Noisy Reference Signals	266
10.5	Displaying Waveforms of Tri-State Signals	267
10.6	Getting Help	268
10.7	Shaping the Appearance of Graphic Objects	268
10.8	Suggestions for Case Studies	269
Chapter 11. All-Digital PLLs (ADPLLs)		271
11.1	ADPLL Components	271
11.1.1	All-digital phase detectors	271
11.1.2	All-digital loop filters	277
11.1.3	Digital-controlled oscillators	282
11.2	Examples of Implemented ADPLLs	286

11.3	Theory of a Selected Type of ADPLL	292
11.3.1	The effects of discrete-time operation	293
11.3.2	The hold range of the ADPLL	298
11.3.3	Frequency-domain analysis of the ADPLL	301
11.3.4	Ripple reduction techniques	303
11.3.5	Higher-order ADPLLs	304
11.4	Typical ADPLL Applications	305
11.5	Designing an ADPLL	307
11.5.1	Case study: designing an ADPLL FSK decoder	307
Chapter 12. Computer-Aided Design and Simulation of ADPLLs		311
12.1	Designing the ADPLL	311
12.2	Simulating ADPLL Performance	313
12.3	Case Studies on ADPLL Behavior	314
Chapter 13. The Software PLL (SPLL)		321
13.1	The Hardware-Software Trade-off	321
13.2	<i>The Feasibility of an SPLL Design</i>	322
13.3	SPLL Examples	323
13.3.1	An LPLL-like SPLL	324
13.3.2	A DPLL-like SPLL	330
13.3.3	A note on ADPLL-like SPLLs	339
Chapter 14. The PLL in Communications		341
14.1	Types of Communications: Baseband and Bandpass	341
14.2	Amplitude Shift Keying	343
14.3	Phase Shift Keying	343
14.3.1	Binary phase shift keying (BPSK)	343
14.3.2	Quadrature phase shift keying	345
14.3.3	Offset quadrature PSK (OQPSK)	346
14.3.4	m-ary PSK	347
14.3.5	Differential PSK (DPSK)	347
14.4	Frequency Shift Keying	348
14.4.1	Binary FSK	348
14.4.2	m-ary FSK	350
14.4.3	Minimum shift keying (MSK) and Gaussian MSK (GMSK)	351
14.5	Quadrature Amplitude Modulation (QAM)	355
14.6	The Role of Synchronization in Digital Communications	356
14.7	Digital Communications Using BPSK	357
14.7.1	Transmitter considerations	357
14.7.2	Receiver considerations	362
14.8	Digital Communications Using QPSK	372
14.8.1	Transmitter considerations	372
14.8.2	Receiver considerations	373
14.9	Digital Communications Using QAM	375
14.10	Digital Communications Using FSK	377
14.10.1	Simple FSK decoders: easy to implement, but not effective	377
14.10.2	Coherent FSK detection	379
14.10.3	Noncoherent FSK detection and quadrature FSK decoders	380
14.11	Digital Communications in Mobile Phones	381
14.12	Bandwidth Efficiency, Bit Error Rate (BER), and the Signal Power Efficiency of Digital Modulation Schemes	382

Chapter 15. Searching PLL Integrated Circuits	385
Appendix A. The Pull-in Process	389
A.1 The Simplified Model for the Pull-in Range $\Delta\omega_p$ of the LPLL	389
A.2 A Simplified Model for the Pull-in Time T_p of the LPLL	396
A.3 The Pull-in Range $\Delta\omega_p$ of the DPLL	399
A.4 The Pull-in Time T_p of the DPLL	401
Appendix B. The Laplace Transform	403
B.1 Transforms Are the Engineer's Tools	403
B.2 Laplace Transform Is the Key to Success	406
B.3 A Numerical Example of the Laplace Transform	410
B.4 Some Basic Properties of the Laplace Transform	413
B.4.1 Addition theorem	413
B.4.2 Multiplication by a constant factor k	414
B.4.3 Multiplication of signals	414
B.4.4 Delay in the time domain	415
B.4.5 Differentiation and integration in the time domain	415
B.4.6 The initial- and final-value theorems	419
B.5 Using the Table of Laplace Transforms	420
B.6 Applying the Laplace Transform to Electric Networks	420
B.7 Closing the Gap Between the Time Domain and the Complex Frequency Domain	424
B.8 Networks with Nonzero Stored Energy at $t = 0$	425
B.9 Analyzing Dynamic Performance by the Pole-Zero Plot	426
B.10 A Simple Physical Interpretation of "Complex Frequency"	429
Appendix C. Digital Filter Basics	431
C.1 The Transfer Function $H(z)$ of Digital Filters	431
C.2 IIR Filters	433
C.2.1 The impulse-invariant z -transform	434
C.2.2 The bilinear z -transform	441
C.3 FIR Filters	446
C.3.1 Window-FIR filters	450
C.3.2 Designing FIR filters with the Parks-McClellan algorithm	454
Appendix D. Measuring PLL Parameters	461
D.1 Measurement of Center Frequency f_0	461
D.2 Measurement of VCO Gain K_0	462
D.3 Measurement of Phase-Detector Gain K_d	463
D.4 Measurement of Hold Range $\Delta\omega_H$ and Pull-in Range $\Delta\omega_p$	465
D.5 Measurement of Natural Frequency ω_n , Damping Factor ζ , and Lock Range $\Delta\omega_L$	467
References	473
Index	477