

2793-0868

---

# FUNDAMENTALS OF MODERN VLSI DEVICES

**YUAN TAUR**

**TAK H. NING**



**CAMBRIDGE**  
UNIVERSITY PRESS

---

# CONTENTS

<i>Physical Constants and Unit Conversions</i>	page xi
<i>List of Symbols</i>	xiii
<i>Preface</i>	xxi
<b>1 INTRODUCTION</b>	1
1.1 Evolution of VLSI Device Technology	1
1.2 Modern VLSI Devices	4
1.2.1 Modern CMOS Transistors	4
1.2.2 Modern Bipolar Transistors	5
1.3 Scope and Brief Description of the Book	5
<b>2 BASIC DEVICE PHYSICS</b>	9
2.1 Electrons and Holes in Silicon	9
2.1.1 Energy Bands in Silicon	9
2.1.2 n-Type and p-Type Silicon	12
2.1.3 Carrier Transport in Silicon	19
2.1.4 Basic Equations for Device Operation	24
2.2 p–n Junctions	29
2.2.1 Built-in Potential and Applied Potential	29
2.2.2 Abrupt Junctions	31
2.2.3 The Diode Equation	38
2.2.4 Current-Voltage Characteristics	42
2.2.5 Time-Dependent and Switching Characteristics	50
2.2.6 Diffusion Capacitance	57
2.3 MOS Capacitors	58
2.3.1 Surface Potential: Accumulation, Depletion, and Inversion	58

2.3.2	Electrostatic Potential and Charge Distribution in Silicon	63
2.3.3	Capacitances in an MOS Structure	68
2.3.4	Polysilicon Work Function and Depletion Effects	74
2.3.5	MOS Under Nonequilibrium and Gated Diodes	78
2.3.6	Charge in Silicon Dioxide and at the Silicon–Oxide Interface	82
2.3.7	Effect of Interface Traps and Oxide Charge on Device Characteristics	86
2.4	High-Field Effects	90
2.4.1	Impact Ionization and Avalanche Breakdown	90
2.4.2	Band-to-Band Tunneling	94
2.4.3	Tunneling into and Through Silicon Dioxide	95
2.4.4	Injection of Hot Carriers from Silicon into Silicon Dioxide	97
2.4.5	High-field Effects in Gated Diodes	99
2.4.6	Dielectric Breakdown	100
	Exercises	106
<b>3</b>	<b>MOSFET DEVICES</b>	112
3.1	Long-Channel MOSFETs	113
3.1.1	Drain-Current Model	114
3.1.2	MOSFET $I$ – $V$ Characteristics	117
3.1.3	Subthreshold Characteristics	125
3.1.4	Substrate Bias and Temperature Dependence of Threshold Voltage	129
3.1.5	MOSFET Channel Mobility	132
3.1.6	MOSFET Capacitances and Inversion-Layer Capacitance Effect	135
3.2	Short-Channel MOSFETs	139
3.2.1	Short-Channel Effect	139
3.2.2	Velocity Saturation	149
3.2.3	Channel Length Modulation	154
3.2.4	Source–Drain Series Resistance	158
3.2.5	MOSFET Breakdown	160
	Exercises	161

---

<b>4</b>	<b>CMOS DEVICE DESIGN</b>	164
4.1	MOSFET Scaling	164
4.1.1	Constant-Field Scaling	164
4.1.2	Generalized Scaling	167
4.1.3	Nonscaling Effects	170
4.2	Threshold Voltage	173
4.2.1	Threshold-Voltage Requirement	173
4.2.2	Nonuniform Doping	177
4.2.3	Channel Profile Design	184
4.2.4	Quantum Effect on Threshold Voltage	194
4.2.5	Discrete Dopant Effects on Threshold Voltage	200
4.3	MOSFET Channel Length	202
4.3.1	Various Definitions of Channel Length	202
4.3.2	Extraction of the Effective Channel Length	204
4.3.3	Physical Meaning of Effective Channel Length	211
	Exercises	221
<b>5</b>	<b>CMOS PERFORMANCE FACTORS</b>	224
5.1	Basic CMOS Circuit Elements	224
5.1.1	CMOS Inverters	224
5.1.2	CMOS NAND and NOR Gates	232
5.1.3	Inverter and NAND Layouts	237
5.2	Parasitic Elements	240
5.2.1	Source–Drain Resistance	240
5.2.2	Parasitic Capacitances	244
5.2.3	Gate Resistance	247
5.2.4	Interconnect $R$ and $C$	250
5.3	Sensitivity of CMOS Delay to Device Parameters	257
5.3.1	Propagation Delay and Delay Equation	257
5.3.2	Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness	264
5.3.3	Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage	269
5.3.4	Sensitivity of Delay to Parasitic Resistance and Capacitance	272

8.3.3	Device Optimization When There Is Negligible Base Widening	392
8.3.4	Device Optimization for Small Power-Delay Product	396
8.3.5	Bipolar Device Optimization – An Example	397
8.4	Bipolar Device Scaling for ECL Circuits	398
8.4.1	Device Scaling Rules	399
8.4.2	Limits in Bipolar Device Scaling for ECL Circuits	401
8.5	Bipolar Device Optimization and Scaling for Analog Circuits	404
8.5.1	Optimizing the Individual Parameters	405
8.5.2	Technology for Analog Bipolar Devices	407
8.5.3	Limits in Scaling Analog Bipolar Transistors	408
	Exercises	409
<b>Appendix 1</b>	<b>CMOS PROCESS FLOW</b>	414
<b>Appendix 2</b>	<b>OUTLINE OF A PROCESS FOR FABRICATING MODERN n-p-n BIPOLAR TRANSISTORS</b>	418
<b>Appendix 3</b>	<b>EFFECTIVE DENSITY OF STATES</b>	419
<b>Appendix 4</b>	<b>EINSTEIN RELATIONS</b>	422
<b>Appendix 5</b>	<b>ELECTRON-INITIATED AND HOLE-INITIATED AVALANCHE BREAKDOWN</b>	425
<b>Appendix 6</b>	<b>AN ANALYTICAL SOLUTION FOR THE SHORT-CHANNEL EFFECT IN SUBTHRESHOLD</b>	427
<b>Appendix 7</b>	<b>QUANTUM-MECHANICAL SOLUTION IN WEAK INVERSION</b>	434
<b>Appendix 8</b>	<b>DETERMINATION OF EMITTER AND BASE SERIES RESISTANCES</b>	438
<b>Appendix 9</b>	<b>INTRINSIC-BASE RESISTANCE</b>	443
	<i>References</i>	449
	<i>Index</i>	461