Design Flows
A Power-Aware Online Scheduling Algorithm for Streaming Applications in Embedded MPSoC p. 1
System Level Power Estimation of System-on-Chip Interconnects in Consideration of Transition Activity and Crosstalk p. 21
Residue Arithmetic for Designing Low-Power Multiply-Add Units p. 31

Circuit Techniques 1
An On-chip Flip-Flop Characterization Circuit p. 41
A Low-Voltage Log-Domain Integrator Using MOSFET in Weak Inversion p. 51
Physical Design Aware Comparison of Flip-Flops for High-Speed Energy-Efficient VLSI Circuits p. 62
A Temperature-Aware Time-Dependent Dielectric Breakdown Analysis Framework p. 73

Low Power Circuits
An Efficient Low Power Multiple-Value Look-Up Table Targeting Quaternary FPGAs p. 84
On Line Power Optimization of Data Flow Multi-core Architecture Based on Vdd-Hopping for Local DVFS p. 94
Self-Timed SRAM for Energy Harvesting Systems p. 105
L1 Data Cache Power Reduction Using a Forwarding Predictor p. 116

Self-Timed Circuits
Optimizing and Comparing CMOS Implementations of the C-Element in 65nm Technology p. 137
Self-Timed Ring Case p. 150
Practical and Theoretical Considerations on Low-Power Probability-Codes for Networks-on-Chip p. 160
Process Variation p. 170

Logic Architecture and VDD Selection for Reducing the Impact of Intra-die Random V p. 180
Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis p. 190
Transistor-Level Gate Modeling for Nano CMOS Circuit Verification Considering Statistical Process Variations p. 200
White-Box Current Source Modeling Including Parameter Variation and Its Application in Timing Simulation p. 211

Circuit Techniques 2
Controlled-Precision Pure-Digital Square-Wave Frequency Synthesizer p. 218
An All-Digital Phase-Locked Loop with High Resolution for Local On-Chip Clock Synthesis p. 218
Clock Network Synthesis with Concurrent Gate Insertion p. 228
Modeling Time Domain Magnetic Emissions of ICs p. 238
High-Level Modeling of Power-Aware Heterogeneous Designs in System C-AMS (Abstracts) p. 250
Power Profiling of Embedded Analog/Mixed-Signal Systems p. 250