Portable Pipeline Synthesis for FCCMs p. 1
Performance-Directed Technology Mapping for LUT-Based FPGAs - What Role Do Decomposition and Covering Play? p. 14
FACT: Co-evaluation Environment for FPGA Architecture and CAD System p. 34
An Universal CLA Adder Generator for SRAM-Based FPGAs p. 44
An Emulation System of the WASMII: A Data Driven Computer on a Virtual Hardware p. 55
Custom Computing Machines vs. Hardware/Software Codesign: From a globalized point of view p. 65
The Design of a Coprocessor Board Using Xilinx's XC6200 FPGA - An Experience Report p. 77
RACE: Reconfigurable and Adaptive Computing Environment p. 87
Computing 2-D DFTs Using FPGAs p. 96
CAPpartx: Computer Aided Prototyping Partitioning for Xilinx FPGAs, a Hierarchical Partitioning Tool for Rapid Prototyping p. 106
Architectural Synthesis and Efficient Circuit Implementation for Field Programmable Gate Arrays p. 116
RaPiD - Reconfigurable Pipelined Datapath p. 126
Solving Satisfiability Problems on FPGAs p. 136
FPGA Implementation of the Block-Matching Algorithm for Motion Estimation in Image Coding p. 146
Parallel CRC Computation in FPGAs p. 156
Coherent Demodulation with FPGAs p. 166
The Trianus System and Its Application to Custom Computing p. 176
Logic Synthesis for FPGAs Using A Mixed Exclusive- / Inclusive-OR Form p. 185
Flexible Codesign Target Architecture for Early Prototyping of CMIST Systems p. 193
ATTEMPT-1: A Reconfigurable Multiprocessor Testbed p. 200
A Slow Motion Engine for the Analysis of FPGA-Based Prototypes p. 210
Implementing Reconfigurable Datapaths in FPGAs for Adaptive Filter Design p. 220
A Fast Constant Coefficient Multiplier for the XC6200 p. 230
Key Issues for User Acceptance of FPGA Design Tools p. 237
Reconfigurable DSP Demonstrators for the Development of Spacecraft Payload Processors p. 242
Reconfigurable Logic Based Fibre Channel Network Card With Sub 2 Micro-Second Raw Latency p. 252
An Asynchronous Transfer Mode (ATM) Stream Demultiplexer and Switch p. 260
Optically Reconfigurable FP-GAs: Is this a Future Trend? p. 270
CCSimP - An Instruction-level Custom-Configurable Processor for FPLDs p. 280
Architectural Synthesis Techniques for Dynamically Reconfigurable Logic p. 290
Fast Reconfigurable Crossbar Switching in FPGAs p. 297
Growable FPGA Macro Generator p. 307
Architectural Strategies for Implementing an Image Processing Algorithm on XC6000 FPGA p. 317
A Virtual Hardware Operating System for the Xilinx XC6200 p. 327
An Experimental Programmable Environment for Prototyping Digital Circuits  p. 337
Migration from Schematic-Based Designs to a VHDL Synthesis Environment  p. 346
ASIC Design and FPGA Design: A Unified Design Methodology Applied to Different Technologies  p. 356
FIR Filtering with FPGAs Using Quadrature Sigma-Delta Modulation Encoding  p. 361
A New FPGA Technology Mapping Approach by Cluster Merging  p. 366
An EPLD Based Transient Recorder for Simulation of Video Signal Processing Devices in a VHDL Environment Close to System Level Conditions  p. 371
Convolutional Error Decoding with FPGAs  p. 376
Metastability Characteristics Testing for Programmable Logic Design  p. 381
Implementing Sigma Delta Modulator Prototype Designs on an FPGA  p. 389
Design of a VME Parametrized Library for FPGAs  p. 394
Development of a Telephone Answering Machine in a Lab - FPGAs in Education  p. 400
FPGA Design Migration: Some Remarks  p. 405
Concurrent Design of Hardware/Software Dedicated Systems  p. 410
The Implementation of a Field Programmable Logic Based Co-Processor for the Acceleration of Discrete Event Simulators  p. 415
Computing Weight Distributions of Binary Linear Block Codes on a CCM  p. 425
Author Index  p. 431

Table of Contents provided by Blackwell's Book Services and R.R. Bowker. Used with permission.