Efficient Initial Approximation and Fast Converging Methods for Division and Square Root
Function Evaluation by Table Look-up and Addition
Faithful Bipartite ROM Reciprocal Tables
Analytic Approach for Error Masking Elimination in On-Line Multipliers
Reducing the Number of Counters Needed for Integer Multiplication
Design Strategies for Optimal Multiplier Circuits
Redundant Binary Booth Recoding
Sign Detection and Comparison Networks with a Small Number of Transitions
Application of Fast Layout Synthesis Environment to Dividers Evaluation
The SNAP Project: Towards Sub-Nanosecond Arithmetic
A Complex-Number Multiplier Using Radix-4 Digits
A GaAs IEEE Floating Point Standard Single Precision Multiplier
30-ns 55-b Shared Radix 2 Division and Square Root Using a Self-Timed Circuit
High-Speed Double Precision Computation of Nonlinear Functions
Cascaded Implementation of an Iterative Inverse-Square-Root Algorithm, with Overflow Lookahead
Very-High Radix Combined Division and Square Root with Prescaling and Selection by Rounding
An Area/Performance Comparison of Subtractive and Multiplicative Divide/Square Root Implementations
It Takes Six Ones to Reach a Flaw
167 MHz Radix-4 Floating Point Multiplier
167 MHz Radix-8 Divide and Square Root Using Overlapped Radix-2 Stages
The K5 Transcendental Functions
Redundant CORDIC Rotator Based on Parallel Prediction
High Speed DCT/IDCT Using a Pipelined CORDIC Algorithm
O(n)-Depth Circuit Algorithm for Modular Exponentiation
Simplifying Quotient Determination in High-Radix Modular Multiplication
Semi-Logarithmic Number Systems
Arithmetic for Relative Accuracy
A New VLSI Vector Arithmetic Coprocessor for the PC
Exact Computation of a Sum or Difference with Applications to Argument Reduction
Hardware Design and Arithmetic Algorithms for a Variable-Precision, Interval Arithmetic Coprocessor
An $\epsilon$ Arithmetic for Removing Degeneracies
Additional Paper
Author Index