General Chair's Message
Message from the Steering Committee Chair
Program Chair's Message
Conference Chairs
Keynote Address: 21st Century Gigascale Integration (GSI)
Reviewers List
Panel: Low Power versus High Speed: Can you have both?
Uniform Area Timing-Driven Circuit Implementation p. 2
Optimization Using Implicit Techniques for Industrial Designs p. 8
Optimal Technology Mapping for Single Output Cells p. 14
A Differential Model Approach to Analog Design Automation p. 22
A New Approach for Modeling and Optimization of Analog Systems p. 28
A Scalable Analog Architecture for Neural Networks with On-Chip Learning and Refreshing p. 33
Bus Minimization and Scheduling of Multi-Chip Systems p. 40
Thumbnail Rectilinear Steiner Trees p. 46
A Two-Stage Simulated Annealing Methodology p. 50
Optimizing Wiring Space in Slicing Floorplans p. 54
Estimating Worst-Case Power Consumption of CMOS Circuits Modeled as Symbolic Neural Networks p. 60
Design and Analysis of a Low-Power Energy-Recovery Adder p. 66
Coding a Terminated Bus for Low Power p. 70
Circuit/Architecture for Low-Power High-Performance 32bit Adder p. 74
Symbolic Execution of Data Paths p. 80
Specification and Synthesis of Bounded Indirection p. 86
Synthesis of SEU-Tolerant ASICs Using Concurrent Error Correction p. 90
Scheduling Conditional Data-Flow Graphs with Resource Sharing p. 94
Automated Verification of Temporal Properties Specified as State Machines in VHDL p. 100
Partitioning Transition Relations Efficiently and Automatically p. 106
Using Symbolic Rademacher-Walsh Spectral Transforms to Evaluate the Correlation Between Boolean Functions p. 112
An Efficient Building Block Layout Methodology for Compact Placement p. 118
Performance Driven Standard-cell Placement Using the Genetic Algorithm p. 124
An Efficient Heuristic Approach on Minimizing the Number of Feedthrough Cells in Standard Cell Placement p. 128
Priority Driven Channel Pin Assignment p. 132
A Systolic Algorithm and Architecture for Image Thinning p. 138
Analyzing and Verifying of Locally Clocked Circuits with the Concurrency Workbench p. 144
Automatic Rapid Prototyping of Semi-Custom VLSI Circuits Using Actel FPGAs p. 148
A Local Clocking Approach for Self-timed Datapath Designs p. 152
A Soft Computing Approach to Hardware Software Codesign p. 158