Introductory Issues p. 1
Design of CPU Cache Memories p. 4
Synchronization, Coherence, and Event Ordering in Multiprocessors p. 14
Effects of Cache Coherency in Multiprocessors p. 27
A Survey of Cache Coherence Schemes for Multiprocessors p. 44
Hardware Solutions for Cache Coherence in Shared-Memory Multiprocessor Systems p. 57
Memory Reference Characteristics of Parallel Programs p. 69
A Characterization of Sharing in Parallel Programs and its Application to Coherency Protocol Evaluation p. 72
Memory-Reference Characteristics of Multi-Processor Applications under MACH p. 82
The Effect of Sharing on the Cache and Bus Performance of Parallel Programs p. 93
Directory Cache Coherence Protocols p. 107
Cache System Design in the Tightly Coupled Multiprocessor System p. 111
A New Solution to Coherence Problems in Multicache Systems p. 116
An Economical Solution to the Cache Coherence Problem p. 123
An Empirical Evaluation of Two Memory-Efficient Directory Methods p. 131
Two Economical Directory Schemes for Large-Scale Cache-Coherent Multiprocessors p. 141
Directory-Based Cache Coherence in Large-Scale Multiprocessors p. 150
Snoopy Cache Coherence Protocols p. 161
Using Cache Memory to Reduce Processor-Memory Traffic p. 165
A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories p. 173
Dynamic Decentralized Cache Schemes for MIMD Parallel Processors p. 180
Implementing a Cache Consistency Protocol p. 188
Firefly: A Multiprocessor Workstation p. 196
Multiprocessor Cache Synchronization: Issues, Innovations, Evolution p. 208
Coherency For Multiprocessor Virtual Address Caches p. 218
A Class of Compatible Cache Consistency Protocols and Their Support by the IEEE Futurebus p. 228
Competitive Snoopy Caching p. 238
Coherence in Multilevel Cache Hierarchies p. 249
On the Inclusion Properties for Multi-Level Cache Hierarchies p. 252
Organization and Performance of a Two-Level Virtual-Real Cache Hierarchy p. 260
Cache Coherence Schemes in Large-Scale Multiprocessors p. 269
Hierarchical Cache/Bus Architecture for Shared Memory Multiprocessors p. 273
A Cache Coherence Approach For Large Multiprocessor Systems p. 282
The Wisconsin Multicube: A New Large-Scale Cache-Coherent Multiprocessor p. 291
The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor p. 301
Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes p. 313
LimitLESS Directories: A Scalable Cache Coherence Scheme p. 323
Evaluation of Hardware Cache Coherence Schemes p. 335
<table>
<thead>
<tr>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Simulation Study of Snoopy Cache Coherence Protocols</td>
<td>365</td>
</tr>
<tr>
<td>Evaluating the Performance of Four Snooping Cache Coherency Protocols</td>
<td>375</td>
</tr>
<tr>
<td>An Evaluation of Directory Schemes for Cache Coherence</td>
<td>389</td>
</tr>
<tr>
<td>Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures</td>
<td>399</td>
</tr>
<tr>
<td>An Accurate and Efficient Performance Analysis Technique for Multiprocessor Snooping Cache-Consistency Protocols</td>
<td>411</td>
</tr>
<tr>
<td>Comparison of Hardware and Software Cache Coherence Schemes</td>
<td>419</td>
</tr>
<tr>
<td>About the Authors</td>
<td>431</td>
</tr>
</tbody>
</table>

Table of Contents provided by Blackwell's Book Services and R.R. Bowker. Used with permission.