Sampling from the Multivariate Gaussian Distribution Using Reconfigurable Hardware  p. 3

A Fast FPGA-Based 2-Opt Solver for Small-Scale Euclidean Traveling Salesman Problem  p. 13

On the Acceleration of Shortest Path Calculations in Transportation Networks  p. 23
Enhancing Relocatability of Partial Bitstreams for Run-Time Reconfiguration  p. 35
A Library and Platform for FPGA Bitstream Manipulation  p. 45
A Structural Object Programming Model, Architecture, Chip and Tools for Reconfigurable Computing
Configurable Transactional Memory  p. 65
A Reconfigurable Hardware Interface for a Modern Computing System  p. 73
FPGA Acceleration of Gene Rearrangement Analysis  p. 85
FPGA-Accelerated Seed Generation in Mercury BLASTP  p. 95
Systolic Architecture for Computational Fluid Dynamics on FPGAs  p. 107
FPGA-Based Multigrid Computation for Molecular Dynamics Simulations  p. 117
Reconfigurable Computing Cluster (RCC) Project: Investigating the Feasibility of FPGA-Based Petascale Computing
Efficient Mapping of Dimensionality Reduction Designs onto Heterogeneous FPGAs  p. 141
K-means Clustering for Multispectral Images Using Floating-Point Divide  p. 151
Optimizing Logarithmic Arithmetic on FPGAs  p. 163
Generating FPGA-Accelerated DFT Libraries  p. 173
An FPGA Implementation of Pipelined Multiplicative Division with IEEE Rounding  p. 185
Integer Factorization Based on Elliptic Curve Method: Towards Better Exploitation of Reconfigurable Hardware
Matched Filter Computation on FPGA, Cell and GPU  p. 207
A Data-Driven Approach for Pipelining Sequences of Data-Dependent Loops  p. 219
Writing Portable Applications that Dynamically Bind at Run Time to Reconfigurable Hardware  p. 229
Mitrion-C Application Development on SGI Altix 350/RC100  p. 239
Automatic On-Chip Memory Minimization for Data Reuse  p. 251
Scientific Application Acceleration with Reconfigurable Functional Units  p. 261
Design and Implementation of a Highly Parameterised FPGA-Based Skeleton for Pairwise Biological Sequence Alignment  p. 275
The Case for Dynamic Execution on Dynamic Hardware  p. 279
On Solving RC5 Challenges with FPGAs  p. 281
Operating System Integration and Performance of a Multi Stream Cipher Architecture for Reconfigurable System-on-Chip  p. 283
A Novel Technique to Create Energy-Efficient Contexts for Reconfigurable Logic  p. 285
New Protection Mechanisms for Intellectual Property in Reconfigurable Logic  p. 287
Establishing Chain of Trust in Reconfigurable Hardware  p. 289
Hand-Based Interface for Augmented Reality  p. 291
Discrete-Time Cellular Neural Networks in FPGA  p. 293
Run-Time Mapping and Communication Strategies for Homogeneous NoC-Based MPSoCs  p. 295
Code Compressor and Decompressor for Ultra Large Instruction Width Coarse-Grain Reconfigurable Systems p. 297
Software/Hardware Co-scheduling for Reconfigurable Computing Systems p. 299
Mapping Real Time Operating System on Reconfigurable Instruction Cell Based Architectures p. 301
Abstracting Modern FCCMs to Provide a Single Interface to Architectural Resources p. 305
A Novel Technique to Create Energy-Efficient Contexts for Reconfigurable Logic p. 309
Heterogeneous Floorplanner for FPGA p. 311
Automatic Self-Reconfiguration of System-on-Chip Peripherals p. 313
A Hybrid Memory Sub-system for Video Coding Applications p. 317
Rapid Prototyping of Large-Scale Analog Circuits with Field Programmable Analog Array p. 319
PixelStreams-Based Implementation of Videodetector p. 321
Design Space Exploration for the BLAST Algorithm Implementation p. 323
An Integrated Video Compression, Encryption and Information Hiding Architecture Based on the SCAN Algorithm and the Stretch Technology p. 327
A Configurable Processor Synthesis System p. 331
Low-Cost Stereo Vision on an FPGA p. 333
Methodology and Experimental Setup for the Determination of System-Level Dynamic Reconfiguration Overhead p. 335
Quantifying Effective Memory Bandwidth of Platform FPGAs p. 337
A Flexible Filter Processor for Fading Channel Simulation p. 339
RBoot: Software Infrastructure for a Remote FPGA Laboratory p. 343
Jumble: A Hardware-in-the-Loop Simulation System for JHDL p. 345
Sparse Matrix-Vector Multiplication Design on FPGAs p. 349
Changing Output Quality for Thermal Management p. 353
Hardware/Software Co-design of a Key Point Detector on FPGA p. 355
Author Index p. 357

Table of Contents provided by Blackwell's Book Services and R.R. Bowker. Used with permission.