Breaking down the memory wall for scalable microprocessor platforms p. 3
Code generation in the polyhedral model is easier than you think p. 7
A compiler framework for recovery code generation in general speculative optimizations p. 17
A multi-platform co-array Fortran compiler p. 29
Retargeting JIT compilers by using C-compiler generated executable code p. 41
Adding limited reconfigurability to superscalar processors p. 53
Architectural support for enhanced SMT job scheduling p. 63
Static placement, dynamic issue (SPDI) scheduling for EDGE architectures p. 74
A high-performance SIMD floating point unit for BlueGene/L: architecture, compilation, and algorithm design p. 85
Impact of Java memory model on out-of-order multiprocessors p. 99
Fair cache sharing and partitioning in a chip multiprocessor architecture p. 111
Architectural support for high speed protection of memory integrity and confidentiality in multiprocessor systems p. 123
AC/DC: an adaptive date cache prefetcher p. 135
The earth simulator and beyond - technological considerations toward the sustained petaflops machine p. 149
The energy impact of aggressive loop fusion p. 153
Scalable high performance cross-module inlining p. 165
Decoupled software pipelining with the synchronization array p. 177
Fast paths in concurrent programs p. 189
Compiler estimation of load imbalance overhead in speculative parallelization p. 203
Implementing malleability on MPI jobs p. 215
Partitioning of code for a massively parallel machine p. 225
Polymorphic processors: how to expose arbitrary hardware functionality to programmers p. 239
The value evolution graph and its use in memory reference analysis p. 243
TO-lock: removing lock overhead using the owners' temporal locality p. 255
The stream virtual machine p. 267
An adaptive algorithm selection framework p. 278

Table of Contents provided by Blackwell's Book Services and R.R. Bowker. Used with permission.