Functional Redundancy for Dynamic Exploitation of Performance-Energy Consumption Trade-Offs p. 165
Modeling an E1/TU12 Mapper for SDH Systems p. 171
JPEG Decoding in an Electronic Voting Machine p. 177
Industrial Applications/Applications of FPGAs
An FPGA Implementation of the ATM Layer p. 185
Prototyping a Pager-Like Device Using FPGAs: Design of an Object Finder p. 191
Jet Determination in Liquid Argon Calorimeters Using a Heavily Interconnected System of Field Programmable Gate Arrays p. 197
Digital Design
Hybrid Latch Flip-Flop with Improved Power Efficiency p. 211
SisECO: Design of an Echo-Canceling IC for Base Band Modens p. 216
Modeling of Short Circuit Power Consumption Using Timing-Only Logic Cell Macromodelsp. 222
The Use of Extended TSPC CMOS Structures to Build Circuits with Doubled Input/Output p. 228
Fault Tolerant Design
Evaluation of Soft Error Tolerance Technique Based on Time and/or Space Redundancy p. 237
Optimized Generation of VHDL Mutants for Injection of Transition Errors p. 243
Recent Improvements on the Specification of Transient-Fault Tolerant VHDL Descriptions: A Case-Study for Area Overhead Analysis p. 249
Designing a Radiation Hardened 8051-Like Micro-Controller p. 255
Formal Methods and H/S Co-Design
An ACL2 Model of VHDL for Symbolic Simulation and Formal Verification p. 269
A New Approach to Solving the Hardware-Software Partitioning Problem in Embedded System Design p. 275
Design of a Classification System for Rectangular Shapes Using a Co-Design Environment p. 281
Analog and Mixed-Signal Design
Fault Models and Compact Test Vectors for MOS OpAmp Circuits p. 289
Toward Analog Circuit Synthesis: A Global Methodology Based upon Design of Experiments p. 295
A JAVA-Based Mixed-Signal Design Environment p. 301
Testing Mixed-Signal Cores p. 307
Physical Modeling
What is the Appropriate Model for Crosstalk Control? p. 315
Efficient vMOS Realization of Threshold Voters for Self-Purging Redundancy p. 321
LASCA--Interconnect Parasitic Extraction Tool for Deep-Submicron IC Design p. 327
An Integrated Circuit for the in situ Characterization of CMOS Post-Process Micromachining p. 333
Reconfigurable Hardware
<table>
<thead>
<tr>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>An Application-Tailored Dynamically Reconfigurable Hardware Architecture for Digital Baseband Processing</td>
<td>341</td>
</tr>
<tr>
<td>Exploiting FPGA-Based Architectures and Design Tools for Problems of Reconfigurable Computations</td>
<td>347</td>
</tr>
<tr>
<td>Synthesis of Control Circuits with Dynamically Modifiable Behavior on the Basis of Statically Reconfigurable FPGAs</td>
<td>353</td>
</tr>
<tr>
<td>Implementation of Cryptographic Applications on the Reconfigurable FPGA Coprocessor microEnable</td>
<td>359</td>
</tr>
<tr>
<td>Low-Power, Low-Voltage</td>
<td>365</td>
</tr>
<tr>
<td>Limits to Voltage Scaling from the Low Power Perspective</td>
<td>371</td>
</tr>
<tr>
<td>Adaptive Partial Businvert Encoding for Power-Efficient Data Transfer over Wide System Buses</td>
<td>377</td>
</tr>
<tr>
<td>Energy-Efficient Register Access</td>
<td>383</td>
</tr>
<tr>
<td>Embedded Systems</td>
<td>385</td>
</tr>
<tr>
<td>Design and Simulation of Heterogenous Embedded Systems</td>
<td>391</td>
</tr>
<tr>
<td>A Comparison of OO and Reactive Based Specifications on the Design of Embedded Systems</td>
<td>397</td>
</tr>
<tr>
<td>A Comparison of Microcontrollers Targeted to FPGA-Based Embedded Applications</td>
<td>403</td>
</tr>
</tbody>
</table>

Table of Contents provided by Blackwell's Book Services and R.R. Bowker. Used with permission.