Preface

VLSI Design

Achievements in Microelectronics

VLSI Design Procedure

Self-Testing VLSI Chips

VLSI Testability Design Approaches

VLSI Testability Design Feature

Storage Element State Scan Technique

Level Sensitive Scan Design (LSSD)

Random Access Scan Technique

VLSI Design by Boundary-Scan Technique

Self-Testing VLSI Structured Design

Self-testing VLSI Using Scan Path

Ring VLSI Self-Test

Use of General-Purpose Modules for Self-Test VLSI Design

Self-Testing Microcomputers

Pseudorandom Test Pattern Generators

Pseudorandom Sequences

Generators of Uniformly Distributed Pseudorandom Test Sequences

Pseudorandom Test Pattern Generators

Pseudorandom and Related Sequence Generators

Design of Pseudorandom Test Sequence Generator

Generators of Test Sequences Related to Pseudorandom Sequences

Generation of Weighted Pseudorandom Test Sequences

Random Testing

Concept of Random Testing

Probabilistic Analysis Techniques for Digital Circuits

Fault Detection Probability Estimation

Test Sequence Length Calculation

Methods for Optimal Selection of Input Variable Probabilities

Automatic Search for Optimum Probability

Pseudorandom Testing

Pseudorandom Sequences as the Test Sequences of the Circuit

Estimating Fault Coverage for Random and Pseudorandom Tests

Pseudorandom Test Length Calculation

Structured VLSI Design with Built-In Random and Pseudorandom Tests

Exhaustive Testing

Exhaustive Testing Principles

Complexity of Exhaustive Test Sequence Generator Design

Exhaustive Testing by Preweighted Vectors

Iterative Algorithm for Exhaustive Test Generation
Signature Analysis as a Binary Polynomial Division Algorithm
Structured Design of Signature Analyzers
Quadratic Signature Analyzer Property
Multifunctional Signature Analyzer
Signature Analysis Efficiency
Estimation of Signature Analysis Efficiency
Examination of Error Occurrence in Output Responses of Digital Circuits
Signature Analysis Efficiency Estimation Techniques
Evaluation Techniques for Regular Binary Sequence Signatures
Evaluation of Regular Sequence Signatures
A Technique for Calculating Periodic Sequence Signatures
Fast Signature Calculation Algorithm
Multi-Line Compression Schemes
Design of Parallel Signature Analyzers
Compression in Space and Time
State Count Testing
Universal Module BILBO
Analysis of BILBO-PSA Efficiency
Equivalent PSA Circuits with Internal and External XOR Gates
Estimating PSA Detectability on a Two-Stage Equivalent Circuit
Examining Equivalent PSA Circuits with Internal XOR gates
PSA Efficiency Testing by Software Simulation
PSA Design for VLSI Self Test
An Efficient Parallel Signature Analyzer
An Efficient Two-Stage Parallel Signature Analyzer
Efficiency of a Parallel Signature Analyzer
Two-Stage PSA Design
PSA with T-flip-flops Design and Analysis
Introduction to PSA with T-flip-flops Design
Parallel Signature Analyzer with T-flip-flops as Storage Elements
Efficiency of PSA with T-flip-flops as Storage Elements
Simulation of Parallel Signature Analyzers with T-flip-flops
Signature Testability
Signature Testability Analysis
Signature as a Function of Multiple Variables
Investigation of Signature Properties
Generalized Condition for Signature Testability
Evaluation of Signatures
Analytical Evaluation of Boolean Function Signatures
Calculation of Signatures for Identical Generating Polynomials
Finding Signatures for Reciprocal Polynomials \hspace{1cm} p. 299
Signature Testability of VLSI Chips \hspace{1cm} p. 306
Signature Testability of a Circuit \hspace{1cm} p. 306
Signature Testability of Faults at Primary Nodes of Combinational Circuit \hspace{1cm} p. 310
Signature Testability of Two-Level Combinational Circuits \hspace{1cm} p. 312
Analytic Approach to Evaluating Signatures and Signature Testability of faults by PSA \hspace{1cm} p. 314

Appendix 1 \hspace{1cm} p. 321
Appendix 2 \hspace{1cm} p. 327
References \hspace{1cm} p. 329
Index \hspace{1cm} p. 342

Table of Contents provided by Blackwell's Book Services and R.R. Bowker. Used with permission.