Invited Lecture: Logic Synthesis and Design Verification
Efficient Verification with BDDs Using Implicitly Conjoined Invariants
Parametric Circuit Representation Using Inductive Boolean Functions
An Iterative Approach to Language Containment
BDD-Based Debugging of Designs Using Language Containment and Fair CTL
Reliable Hashing Without Collision Detection
A Tool for Symbolic Program Verification and Abstraction
Symbolic Equivalence Checking
A Decision Algorithm for Full Propositional Temporal Logic
Reachability and Recurrence in Extended Finite State Machines: Modular Vector Addition Systems
Automatic Generation of Network Invariants for the Verification of Iterative Sequential Systems
A Graphical Interval Logic Toolset for Verifying Concurrent Systems
Combining Model Checking and Theorem Proving to Verify Parallel Processes
Verification of a Multiplier: 64 Bits and Beyond
Invited Lecture: Protocol Design for an Automated Highway System
Computing Accumulated Delays in Real-Time Systems
Reachability Analysis of Planar Multi-Linear Systems
An Efficient Algorithm for Minimizing Real-Time Transition Systems
Verification of Timing Properties of VHDL
Alternating RQ Timed Automata
Timed Modal Specification - Theory and Tools
A Mechanically Verified Application for a Mechanically Verified Environment
Verification of Real-Time Systems Using PVS
The Formal Verification of an Algorithm for Interactive Consistency Under a Hybrid Fault Model
Computer-Assisted Simulation Proofs
Invited Lecture: A Verifier and Timing Analyser for Simple Imperative Programs
Efficient Verification of Parallel Real-Time Systems
Delay Analysis in Synchronous Programs
Verifying Quantitative Real-Time Properties of Synchronous Programs
A Modal Logic for Message Passing Processes
Functionality Decomposition by Compositional Correctness Preserving Transformation
On Model-Checking for Fragments of [mu]-Calculus
On-The-Fly Verification with Stubborn Sets
All from One, One for All: On Model Checking Using Representatives
Verifying Timed Behavior Automata with Input/Output Critical Races
Refining Dependencies Improves Partial-Order Verification Methods
Exploiting Symmetry in Temporal Logic Model Checking
Symmetry and Model Checking
Generation of Reduced Models for Checking Fragments of CTL